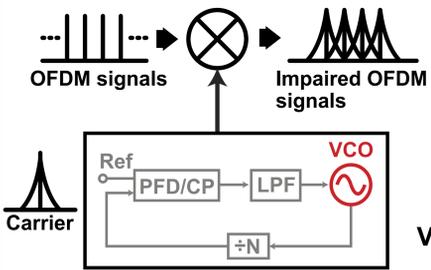


A Tail-Current Modulated VCO with Adaptive-Bias Scheme

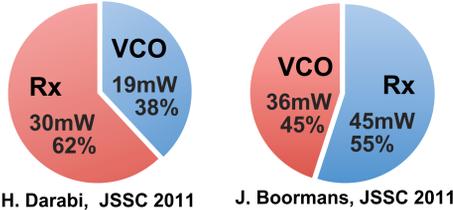
Aravind Tharayil Narayanan, Wei Deng, Kenichi Okada, Akira Matsuzawa
Tokyo Institute of Technology, Japan

1. Research Background

Effects of Phase Noise



Transceiver Power Budget



H. Darabi, JSSC 2011 J. Boormans, JSSC 2011

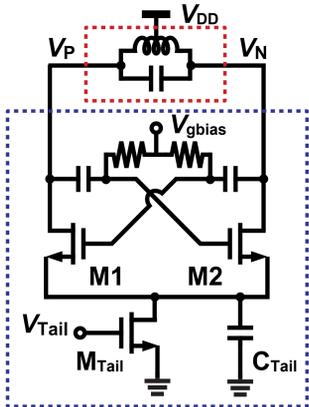
Voltage Controlled Oscillator (VCO)

- Significantly affects TRx noise performance.
- One of the most power hungry TRX building blocks.

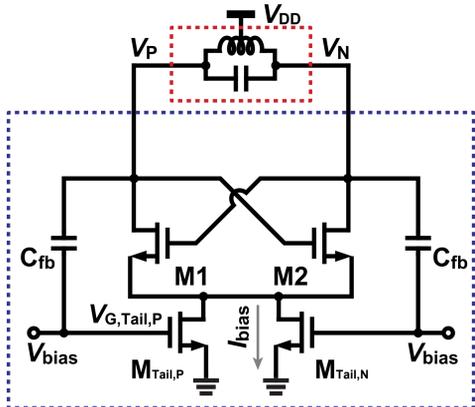
AIM: High performance VCO with minimum area/power overhead.

2. Design for High Performance

Class-C VCO



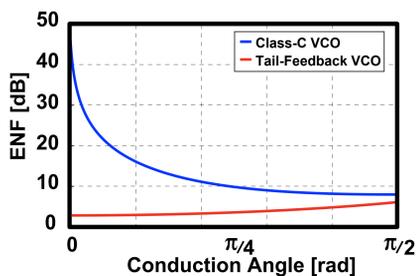
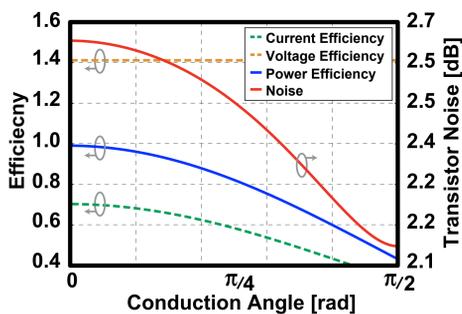
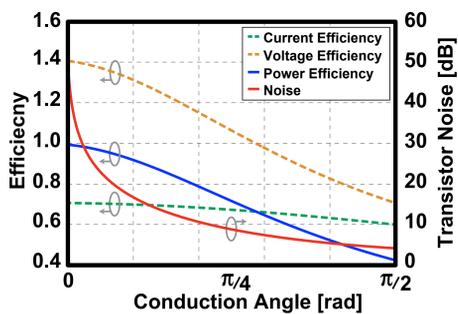
Tail-Feedback VCO



$$ENF = FoM_{MAX} - FoM \quad \text{FoM}_{MAX} = 174 + 10\log(2Q^2)$$

$$ENF = \frac{1 + N_{L,tr}/N_{L,tank}}{\eta_p}$$

- Isolating the noise generated by active circuitry facilitates fair comparison of various VCO architectures.



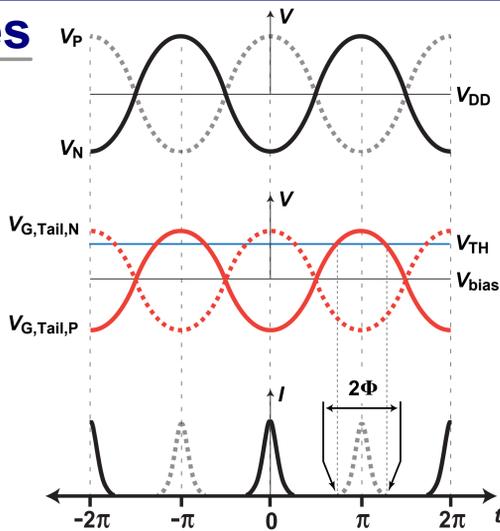
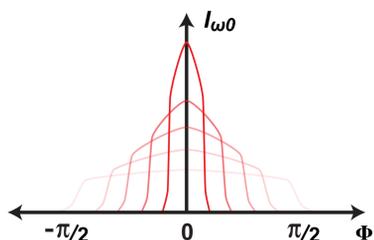
Class-C VCO

- Small Φ results in larger transistor noise.

Tail-Feedback VCO

- Φ can be reduced without increasing transistor noise.

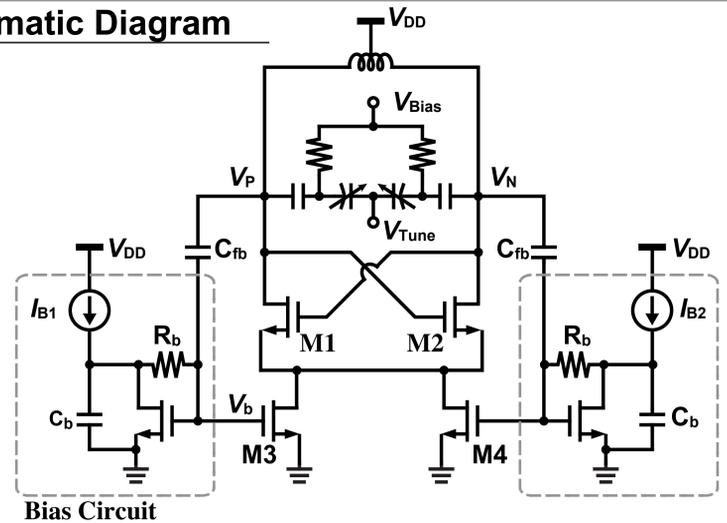
3. Reliability Issues



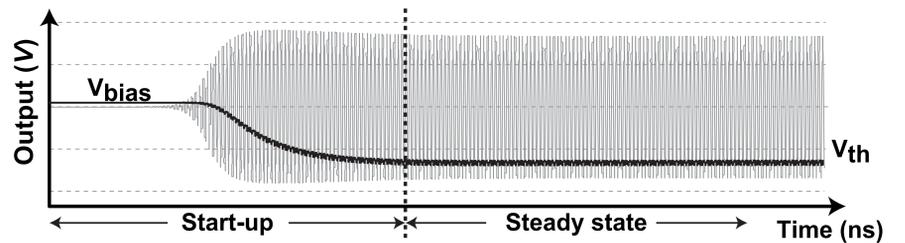
- Small Φ required for high efficiency.
- V_{bias} must be reduced for small Φ .
- VCO fails to start-up at low V_{bias} . i.e. $V_{bias} < V_{th}(M_{TAIL,P}/M_{TAIL,N})$

4. Proposed VCO with Adaptive-Bias

Schematic Diagram

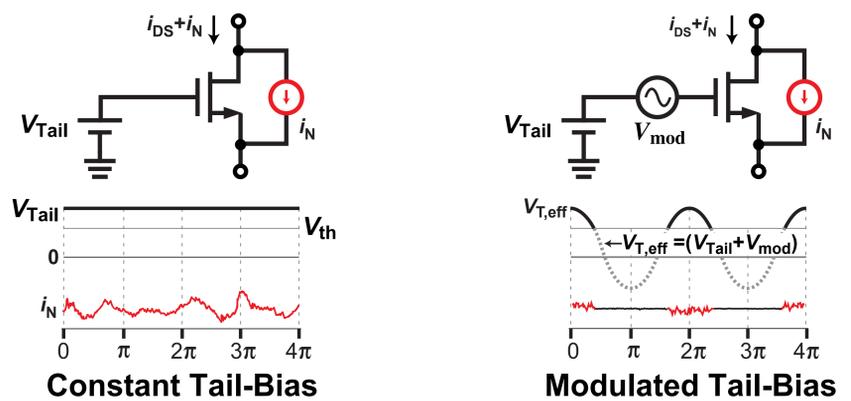


Simulation Results



- High V_{bias} ($>V_{th}$) during start-up.
- V_{bias} is gradually reduced for optimum enhancing efficiency.

5. Tail-Noise Suppression

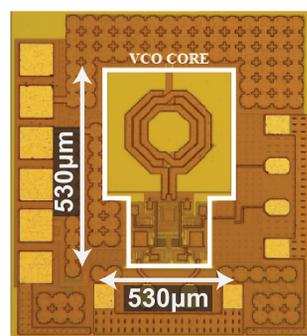


6. Results and Conclusions

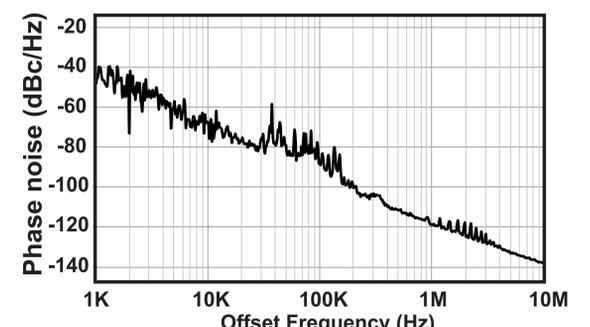
- The proposed adaptive start-up scheme achieves:
 - Reliable start-up.
 - Enhanced DC-RF conversion efficiency.
- These goals are achieved with very little overhead.

	CMOS Process	Frequency[GHz]	Phase Noise [dBc/Hz]	Pdc[mW]	FoM [dBc/Hz]
JSSC2006	250nm	1.75	-125@1MHz	2.25	-186
VLSI2009	180nm	4.50	-109@1MHz	0.16	-190
JSSC2013	180nm	4.84	-125@1MHz	3.40	-193
This Work					
Simulation	180nm	4.80	-124@1Mhz	7.20	-189
Measurement	180nm	4.60	-119@1MHz	6.80	-184

Performance comparison.



Chip micrograph.



Phase noise plot.