A Dual-loop Injection-locked PLL with All-digital Background Calibration System for On-chip Clock Generation

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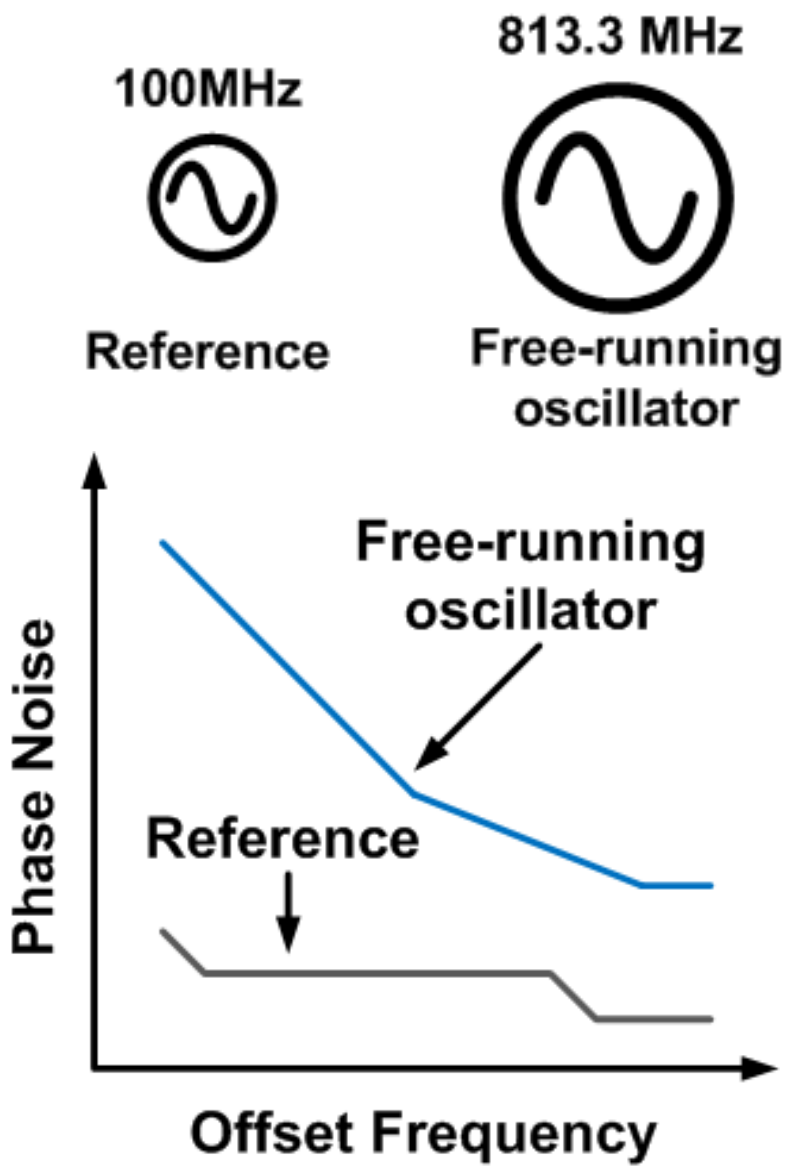
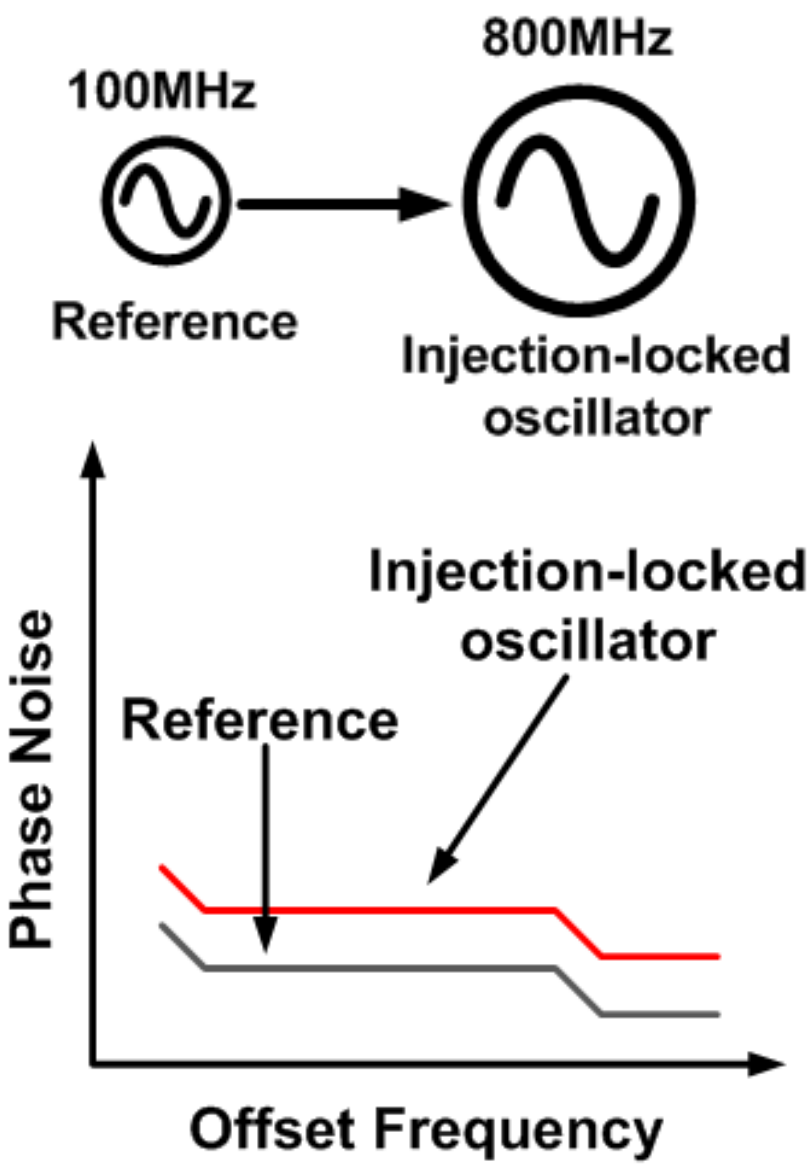
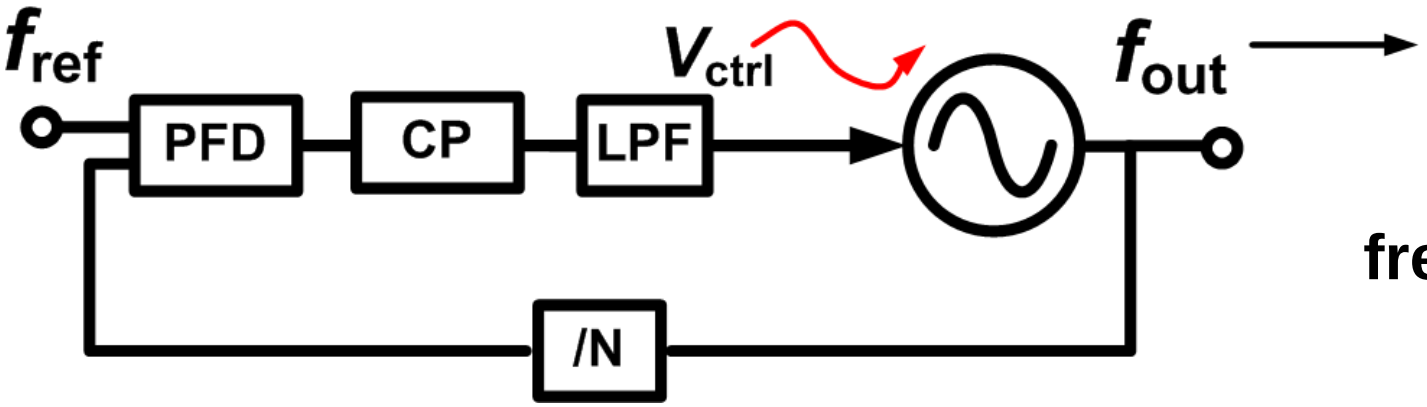
Injection-Locking Technique



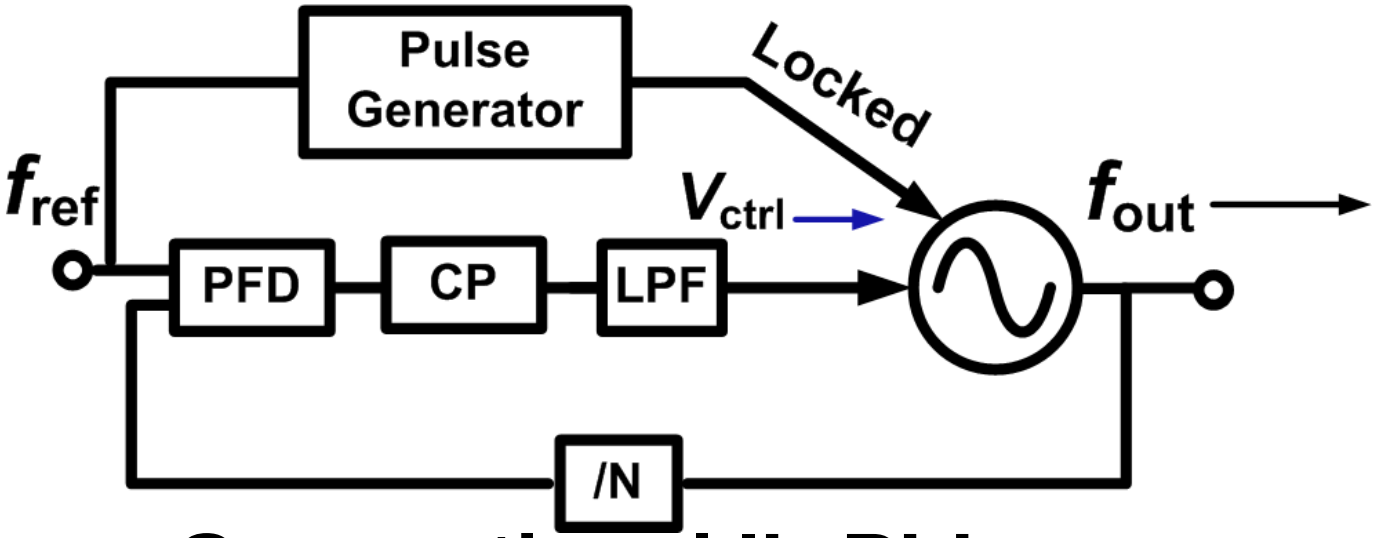


Issue of Injection-locked PLL



Conventional PLL

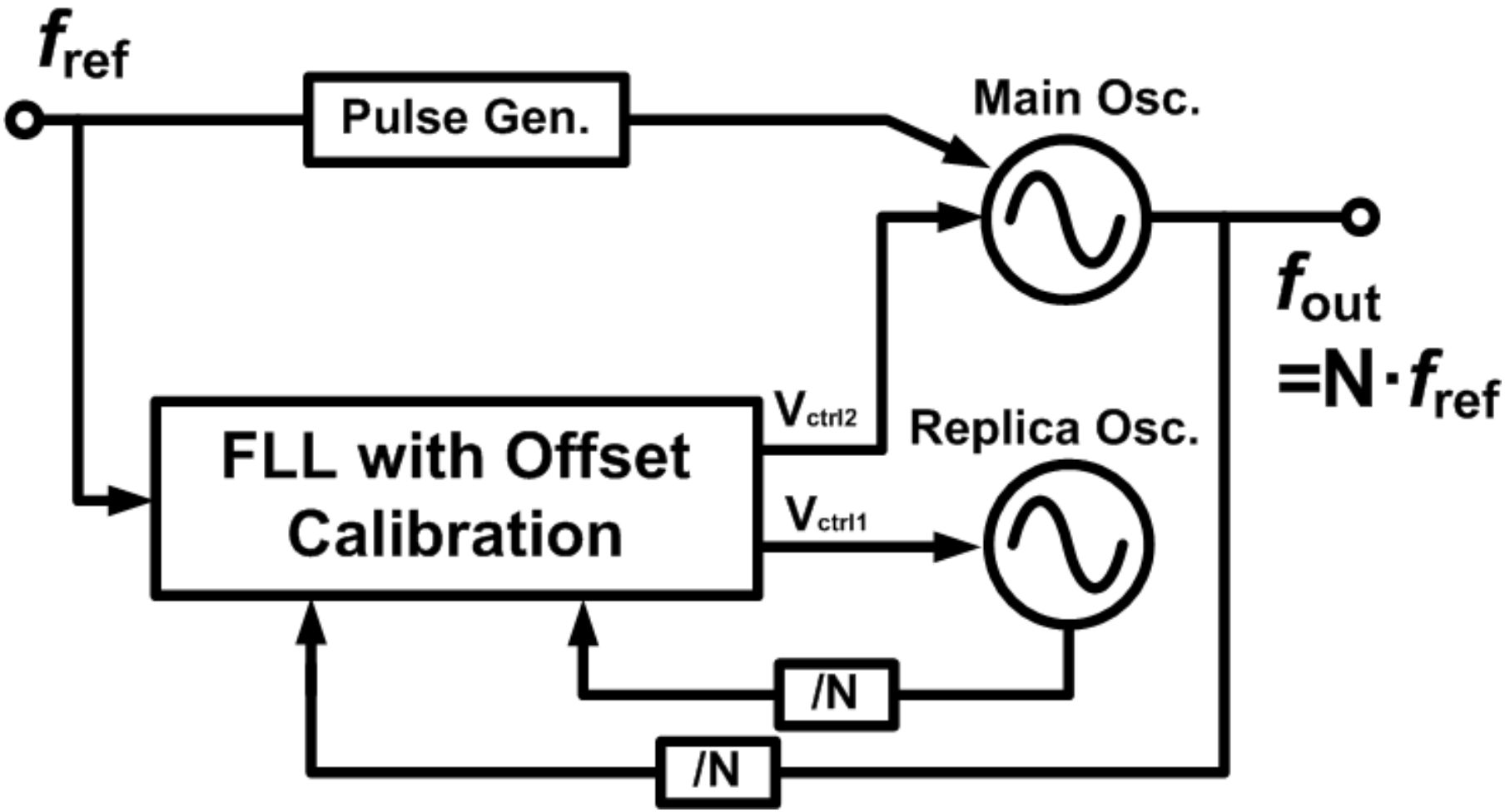
Can track frequency drift



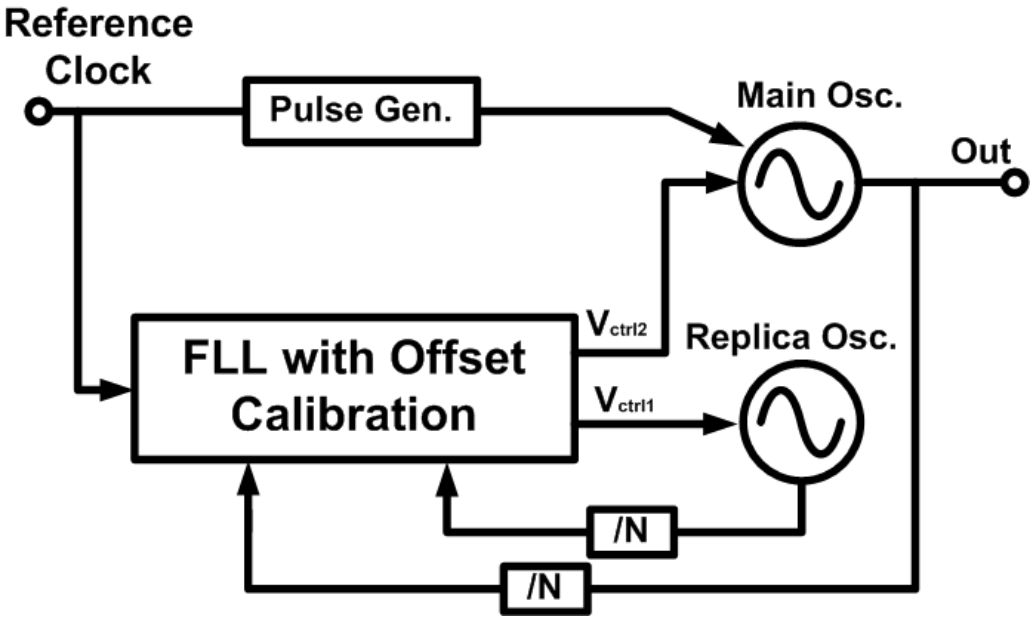
Conventional IL-PLL

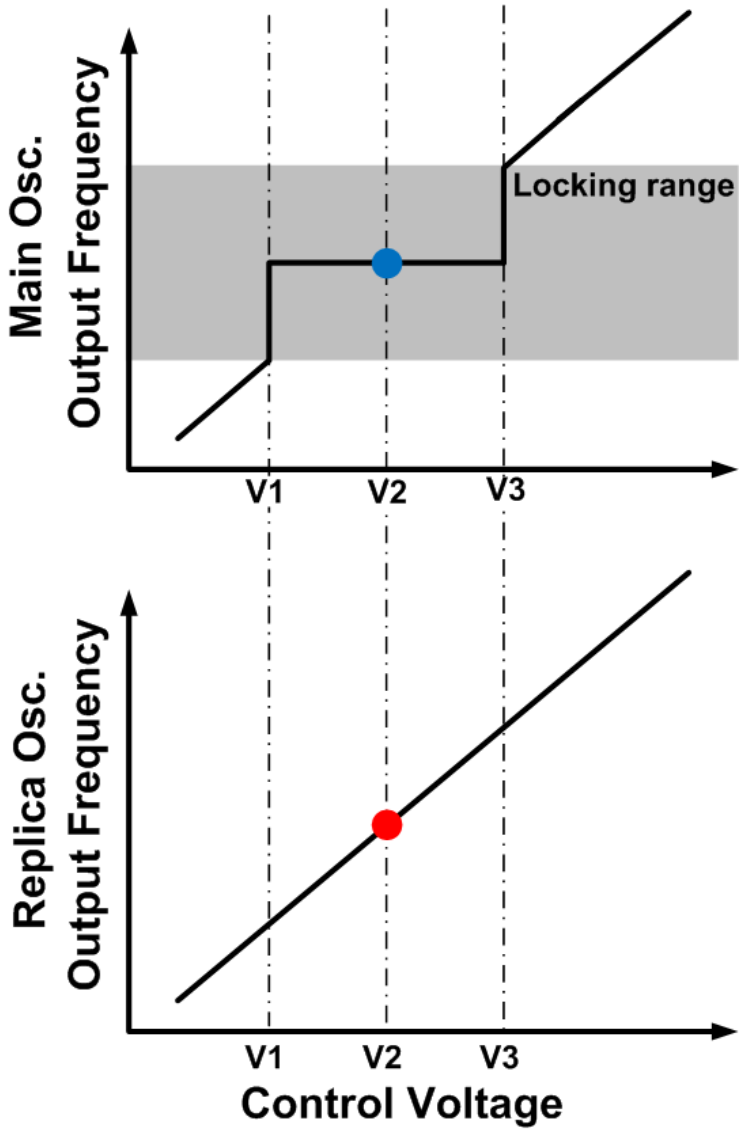
Cannot track frequency drift

Proposed Dual-loop Architecture



PVT Tracking Capability





Performance Comparison

Ref.	[1]		[2]	[3]	This Work
Power [mW]	0.89	1.35	12	6.9	0.97
Area [mm^2]	0.25	0.25	0.058	0.03	0.0022
Integ. Jitter [pS]	0.4	3.2	0.68	2.4	0.7
FOM [dB]	-249	-229	-234	-225	-243

[1] A. Elshazly, *et al*., ISSCC 2012 [2] B. Helal, *et al*., JSSC 2008 [3] C. Liang, *et al*., ISSCC 2011

- **The proposed dual-loop IL-PLL with PVT calibration system can be well suited for low-jitter and small-area clock generation.**