# A Current-Reuse Class-C VCO using Dynamic Start-up Circuits

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## 1. Introduction

Classical LC-based VCOs, *i.e.*, NMOS and CMOS VCOs have been a standard choice for RF circuit design. As shown in Fig.1, CMOS VCO shares the same maximum theoretical phase noise figure-of-merit comparing to NMOS VCO. When operating a CMOS VCO in the current limited region, it can provide 6dB better in FoM comparing to NMOS counterpart providing same power budget and resonator. Additionally, the oscillation swing is within the supply rail which alleviates the reliability issue. More importantly, a current-reuse VCO, which is composed only a pair of NMOS and PMOS, conducts current only half that of CMOS VCO which make it possible to achieve same theoretical phase noise FoM at half power consumption [1].

## 2. Circuit Design and Implementation

Due to higher DC-RF current conversion efficiency, Class-C VCOs can provide a theoretical 3.9dB improvement in FoM comparing to conventional Class-B VCOs [2]. Similar to conventional class of VCOs, a Current-Reuse Class-C VCO can theoretically achieve same low phase noise FoM at the lowest power consumption [3]. As shown in Fig.2, the core VCO is composed of a cross-coupled pair of NMOS and PMOS transistors. The dynamic start-up circuits are composed of two modified current mirrors which provide robust startup and enhance oscillation swing. Moreover, the proposed topology inherently achieves symmetric amplitude through undistorted dynamic current in class-C operation without any additional components that reduces oscillation swing headroom.

The circuit operation can be described as follows. Before the VCO starts to oscillate, the initial gate biases of NMOS and PMOS transistors are determined by  $I_{REF}$ . Once the current in the core oscillator provides enough transconductance to meet startup condition, output starts to swing across  $V_{CM}$ . Then, the adaptive bias scheme acts like a negative feedback which senses an oscillation swing and adaptively changes gate biases of PMOS to be higher and NMOS to be lower to enhance the maximum oscillation swing in a current-limited regime at the steady state.

### 3. Measurement results

The proposed circuit is fabricated in a 180-nm CMOS process. The die micrograph is shown in Fig.3. The measured phase noise is given in Fig.4. The measured tuning range is 4.5GHz to 4.6GHz. For 1.5-V supply, a phase noise of -119dBc/Hz at 1MHz offset can be achieved while consuming 1.6mA which is approximately a figure of merit of -189 dBc/Hz.

## 4. Conclusion

In this paper, a current-reuse class-C VCO using dynamic startup circuits is proposed. The proposed dynamic start-up circuits keep both transistors in a proper operation for high current efficiency and a balanced tank waveform.

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Figure 1: Theoretical FoM limit of conventional class of VCOs and its corresponding Class-C VCOs.



Figure 2: Proposed current-reuse class-C VCO using dynamic startup circuits.



Figure 3: Chip Photograph



Figure 4: Measured phase noise at 4.6 GHz

#### References

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