A Constant-Current-Controlled Class-C VCO using a Self-Adjusting Replica Biasing Scheme

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***Abstract*—This paper proposes a constant-current-controlled class-C VCO using a self-adjusting replica biasing scheme. The proposed class-C VCO can maintain constant current which is more robust over a variation of low gate bias of a cross-coupled pair comparing to a traditional current mirror. The proposed VCO is implemented in a 0.18-µm CMOS process. The measured phase noise is -121.3dBc/Hz at 1MHz offset with a power dissipation of 4.8mW while oscillating at the frequency of 4.9GHz. The figure-of-merit is approximately –189 dBc/Hz.**

Keywords—Class-C; CMOS; constant-current-control: PVT; start-up; VCO

I. INTRODUCTION

The performance of wireless and wireline communication systems is often determined by the phase noise performance of voltage-controlled oscillators (VCOs). More importantly, to satisfy the request for an extension of battery life, power consumption should be kept at its minimum. From recent publications, there have been several techniques to improve phase noise performance based on the traditional class-B LC-tank VCOs *e.g.* noise filter [1], transformer feedback [2], gate-to-source feedback Colpitts VCO [3]. Recently, Andreani, *et al.* introduced a class-C harmonic VCO which exploits the advantages of biasing cross-coupled transistors in class-C operation, resulting in higher DC-RF current conversion efficiency. This contributes to a possibility of saving as much as 36% of power for the same phase noise performance by operating the VCO in class-C instead of traditional class-B [4].

In order to achieve lower phase noise, higher oscillation amplitude of an oscillator is desired. For a class-C operation, the oscillation swing of the VCOs is restricted by gate bias voltage of cross coupled pair (V_{bias}) since the switching pair should not operate in the deep triode region. A lower V_{bias} is desired to increase maximum oscillation swing. However, this poses an oscillation start-up issue since the current in core VCO is heavily decreased at low gate bias V_{bias}. Therefore, the VCO cannot provide enough transconductance to meet the oscillation criteria.

Several approaches have been introduced to improve the start-up issue in class-C VCOs. For example, Okada *et al.* proposes a dual-conduction class-C CMOS VCO [5]-[6] and later utilized in [7], which is a hybrid architecture using a class-B switching pair in parallel to class-C core for a robust start-up.

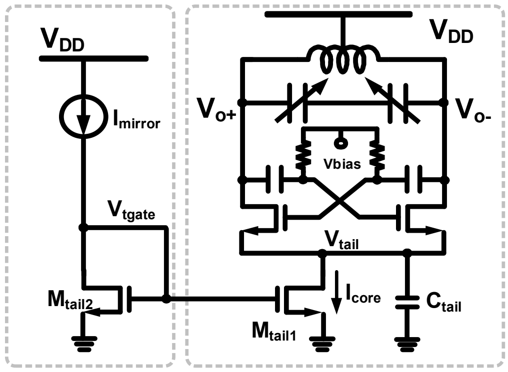

Fig.1. Conventional class-C VCO with traditional current mirror

Different techniques have been proposed by means of negative feedback to adaptively adjust V_{bias} higher at the initial state to provide enough transconductance for a robust startup [8]-[12]. However, a drawback of the approaches in [5]-[6] and [8]-[10] is that the VCO tank is loaded by parallel circuits resulting in degradation of tank quality factor. An approach in [11] generates an adaptive V_{bias} by means of an elegant current mirror but there is a concern for robustness of current control since there is a large difference in drain nodes of current mirror and output oscillation swing. Recently, Fanori and Andreani have proposed two dynamic bias scheme for class-C VCO, *i.e.*, with tail current (F-VCO) and tail resistor (G-VCO), which does not load the tank by sensing the voltage at common source of switching pair and adaptively adjust V_{bias} at the gate cross-coupled pair to keep the same common-node voltage as reference voltage [12]. For G-VCO, reference voltage, however, should be properly chosen and a precise voltage reference is required since any drift in voltage variation can change V_{bias} and current consumption. For a high integration density, a large current source is replaced by tail resistor in F-VCO for more compact area but it raises a concern for current mismatch. High DC gain of the op-amp is also necessary to avoid an inaccuracy of current control and, as well as, modulation of oscillation amplitude. Above negative feedback techniques in class-C VCO [8]-[12], despite of its start-up robustness, the current consumption in the VCO core is poorly defined and sensitive to the parameters in the feedback loop.

This paper proposes an alternative approach to provide robustness over PVT variation at low V_{bias} using a self-adjusting replica biasing scheme. Unlike the traditional current

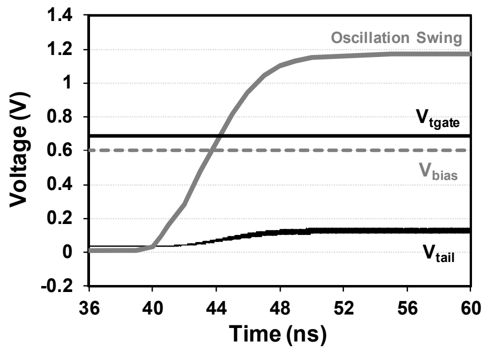

Fig.2. Simulated transient waveforms at specific nodes of class-C VCO with traditional current mirror

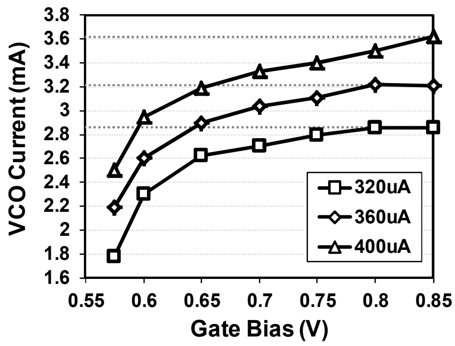

Fig.3. Current consumption of class-C VCO with traditional current mirror at different V_{bias} providing 3 different I_{mirror}

mirror that suffers from significant current reduction at a low V_{bias}, this work utilizes a class-C VCO with a constant current control by means of an adaptive gate bias at the tail transistor which is more suitable for real-life application.

This paper is organized as follows: Section II discusses the issue of conventional class-C VCO with a traditional current mirror. Then, the proposed VCO with a self-adjusting replica biasing scheme for a constant current control is introduced and compared with traditional current mirror. Section III describes the measurement results. Finally, the conclusion is summarized in Section IV.

II. DESIGN OF THE PROPOSED CLASS-C VCO

A. Class-C VCO with Traditional Current Mirror

A Class-C VCO with a traditional current mirror is shown in Fig.1. Fig.2 shows simulated transient waveform of most relevant nodes in the conventional circuit in Fig.1. The simulation results in Fig.2 and Fig.3 are performed with a current mirror ratio of 10. Oscillation swing and common source node of VCO cross-coupled pair (V_{tail}) gradually increase after the startup condition is met at the initial state. Note that a traditional current mirror can only provide a constant gate bias for M_{tial1}. Since there is a large difference in voltages at drains of M_{tial2} and M_{tail1}, the current in VCO (I_{core}) cannot perfectly track the reference current (I_{mirror}). Furthermore, for class-C operation, a low V_{bias} is preferred in order to enhance oscillation swing. This, however, makes V_{tail} significantly decreases comparing to the case when a high V_{bias} is applied and, thus, the current in the VCO greatly diminishes by approximately 30-40% as V_{bias} is varied to 0.575V as shown in Fig.3. Additionally, it raises a concern for an oscillation start-up and a difficulty to determine a bias for optimum performance. More importantly, constant current over variation of V_{bias} is required in the design of a highly-precise bandgap

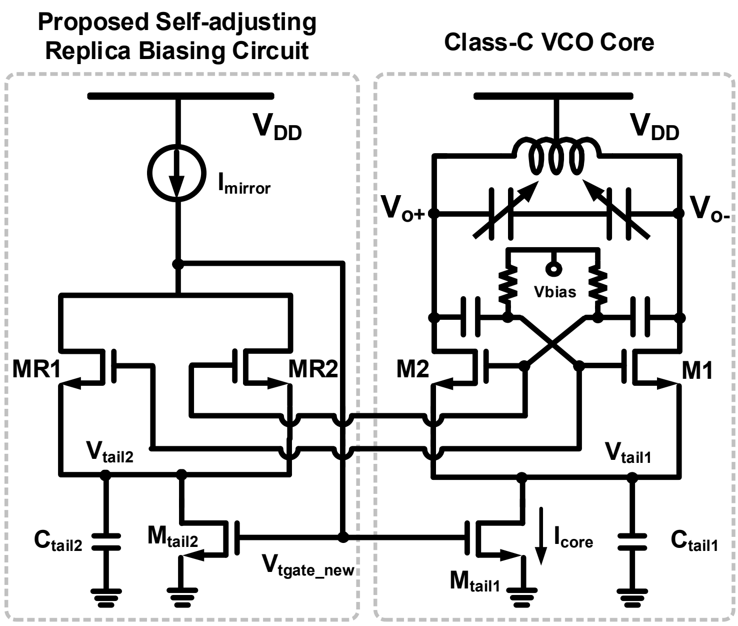

Fig.4. Proposed Class-C VCO with a self-adjusting replica biasing circuit

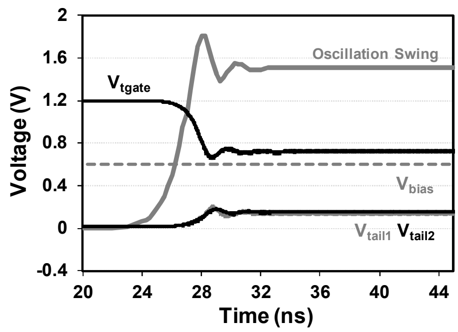

Fig.5. Simulated transient waveform at specific nodes of proposed class-C VCO with self-adjusting replica biasing

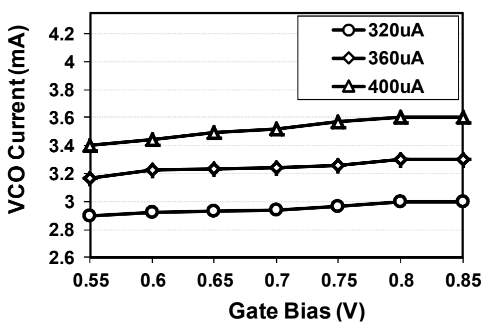

Fig.6. Current consumption of class-C VCO with adaptive replica tail bias at different V_{bias} providing 3 different I_{mirror}

reference voltage. As a result, this makes a class-C VCO with a conventional current mirror not suitable for real-life application due to any voltage variation can cause the class-C VCO fail to oscillate or operate at a sub- optimum performance.

B. Proposed Class-C VCO with a Self-Adjusting Tail Bias Scheme

The proposed class-C VCO with a self-adjusting replica bias circuit is depicted in Fig.4. The adaptive tail bias circuit is composed of replica transistors MR1 and MR2 stacked on top of M_{tail2}. The gates of MR1 and MR2 are tied to gates of M1 and M2 in order to sense V_{bias} and form a duplicate of the VCO cross-coupled pair. Tail transistor M_{tail2} and replica transistors MR1-MR2 are sized with a ratio of 10 smaller than that of M_{tail1} and M1-M2. Unlike conventional case, the common-node of replica pair V_{tail2} can perfectly track V_{tail1} as shown in Fig.5. As a result, when a low V_{bias} is applied, a decrease in V_{tail1} can also be affected in the replica pair. For a constant current flowing in adaptive tail bias circuit, the gate voltage of M_{tail2} (V_{tgate_new}) should increase. In this work, a self-adaptive loop is formed by the connecting gate of M_{tail2} to drain of replica pair.

As shown in Fig.5, at initial state, V_{tail1} and V_{tail2} are low, high V_{tgate_new} are generated through an adaptive loop so that the bias circuit can supply the current to match I_{mirror}. Once oscillation starts up, V_{tail1} and V_{tail2} are relatively higher, V_{tgate_new} are adaptively lowered to maintain a constant current I_{mirror}. This causes current in the replica pair and mirrored current to the core VCO to remain nearly constant before and after the oscillation startup. As shown in Fig.6, from different I_{mirror}, less than 5% decrease of current in the core VCO is observed when 0.55V of V_{bias} is applied which is a large improvement comparing to using a traditional bias circuit in the previous section.

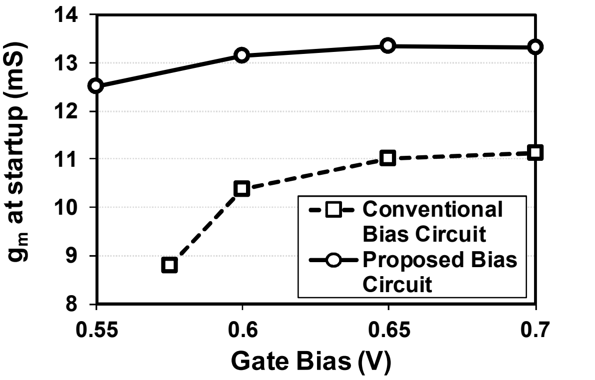

Fig.7. A comparison of simulated small signal g_m variation over V_{bias} of the VCO using traditional and proposed bias circuit with I_{mirror} of 320μA

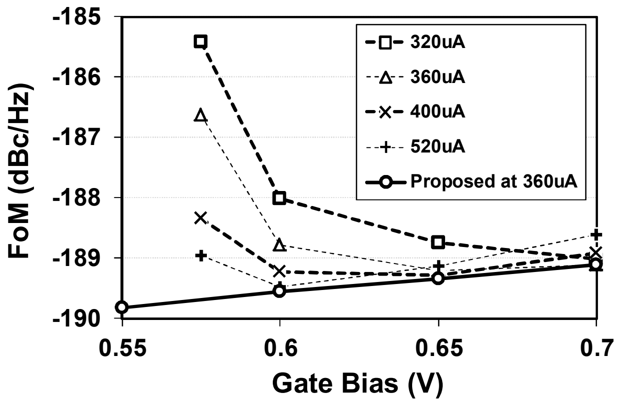

Fig.8. Comparison of FoM of the proposed class-C VCO with adaptive replica biasing circuit at reference current of 360μA and class-C VCO using traditional current mirror at different reference

C. Comparison of Traditional and Proposed Work

It can be seen that the proposed class-C VCO with a self-adjusting replica biasing scheme can provide nearly constant current even at low V_{bias}. This also implies that, for the same reference current I_{mirror}, the proposed work can provide constantly high transconductance (g_m) without the effect of low $V_{bias.}$ On the other hand, the g_m at startup of class-C VCO cross-coupled pair using a traditional bias circuit gradually decreases as V_{bias} reduces. Moreover, when lowering V_{bias} less than 0.575V, the VCO fail to oscillate. The proposed work can be maintained g_m at startup higher than 12 mS and V_{bias} can be as low as 0.55V as shown in Fig.7.

Fig. 8 shows a comparison of the figure-of-merit (FoM) of the class-C VCOs with a traditional current mirror and a proposed adaptive tail gate bias. The FoM is defined as:

$$\mathrm{FoM} = \mathcal{L}(f_{\mathrm{offset}}) - 20\log\left(\frac{f_0}{f_{\mathrm{offset}}}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right) \quad (1)$$

where $L(f_{offset})$ is phase noise, f_{offset} is offset frequency, f_0 is oscillation frequency and P_{DC} is power consumption. It can be seen that, for a class-C VCO using traditional current mirror, 1-3 dB FoM degradation can be observed as V_{bias} is decreased from 0.6 to 0.575 at different I_{mirror}. Since a bandgap reference cannot be applied in a non-constant current control circuit, a small voltage variation at low V_{bias} can cause significant degradation in VCO performance or even a failure to oscillate. Moreover, an optimum current for an optimum phase noise performance should be carefully chosen. The proposed circuit can provide a straight trend for FoM performance as V_{bias} is reduced, since oscillation swing is enhanced at a constant current consumption from I_{mirror} of 360μA. Thus, the figure-of-merit is steadily improved to approximately -190dBc/Hz as V_{bias} reaches 0.55V. This shows an improved robustness over voltage variation and more suitable for real-life application.

III. Measurement Results

To validate the analysis and design in Section II B, the VCO is implemented in a standard 0.18μm CMOS process. Fig.9 shows the micrograph of the fabricated VCO. The core

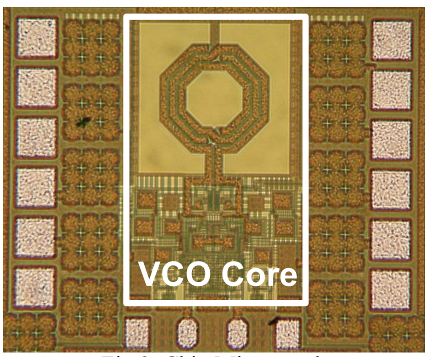

Fig.9. Chip Micrograph

TABLE I

COMPARISON WITH THE-STATE-OF-THE-ART CLASS-C VCOS

Ref.	CMOS Tech.	VCO Topology	Frequency (GHz)	Phase Noise (dBc/Hz)	Power (mW)	FoM	Constant Current Control
[13]	180nm	Capacitive Feedback + FBB	5.6	-118@1MHz offset	3.0	-189	-
[7]	55nm	Class-B/Class-C (Hybrid)	3.95	-137 @2MHz offset	27	-189	No
[5]	180nm	Class-C (Dual)	4.5	-109@1MHz offset	0.16	-190	No
[6]	180nm	Class-C (Improved Dual)	5.4	-113@1MHz offset	0.63	-190	No
[10]	180nm	Class-C (Digital)	3.1	-123@1MHz offset	1.57	-191	No
[8,9]	180nm	Class-C (Single)	4.8	-122@1MHz offset	3.5	-190	No
		Class-C (Feedback)		-125@1MHz offset	3.4	-193	No
[12]	180nm	Class-C (Dynamic)	4.0	147@10MHz offset	6.6	-191	No
This	180nm	**Class-C VCO (Self-adjusting replica bias)**	4.9	-121.3@1MHz offset	4.8	-189	**Yes**

area of the VCO is $0.21mm^2$. The measured tuning range is 4.8 to 4.9 GHz. For 1.2V supply, a phase noise of -121.3dBc/Hz @1MHz offset can be achieved while consuming 4.8mW which is approximately a figure of merit of -189 dBc/Hz.

Table I shows a comparison of the proposed class-C VCO and other state-of-the-art VCOs. The proposed VCO shows a comparable performance with the state-of-the-art conventional class-C VCO in terms of FoM. Even though the feedback class-C VCO [8]-[12] shows a few dB better in FoM as lower V_{bias} can be achieved after oscillation startup, in terms of constant current control, the feedback class-C VCO [8]-[12] requires a proper and precise reference voltage in the feedback loop. A variation of this voltage can alter the current and performance of the class-C VCO. Thus, the proposed class-C VCO has a more constant current control using a self-adjusting bias circuit. Moreover, comparing to the traditional current mirror in class-C VCO, this work is more suitable in real-life application since it is less sensitive to a variation of low V_{bias} which can maintain its operation at an optimum performance.

IV. CONCLUSION

This paper proposes a class-C VCO using a self-adjusting replica biasing scheme. It can provide constant current control even at a variation of low gate bias of a cross-coupled pair. This makes it more suitable for real-life application since its performance is less sensitive over an environmental variation.

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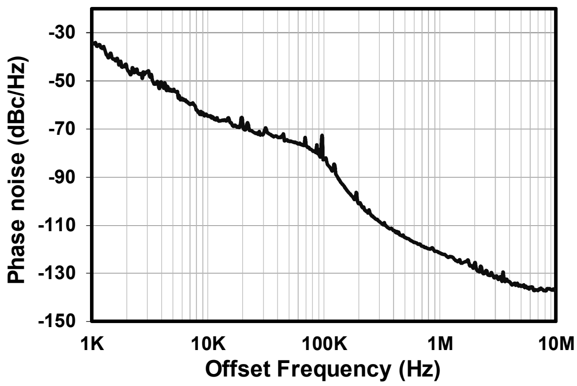

Fig.10. Measured phase noise characteristics at 4.9GHz

REFERENCES

[1] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS LC-oscillator with quadrature outputs," *IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers,* pp.392-393, Feb 1996.

[2] K. Kwok, and H. C. Luong, “Ultra-Low-Voltage High Performance CMOS VCOs Using Transformer Feedback,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 652-660, March 2005.

[3] J.P. Hong and S.G. Lee, “Low phase noise G_m -boosted differential gate-to-source feedback Colpitts CMOS VCO,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3079-3091, Nov. 2009.

[4] A. Mazzanti, and P. Andreani, “Class-C harmonic CMOS VCOs, with a general result on phase noise,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2716-2729, Dec. 2008.

[5] K. Okada, Y. Nomiyama, R. Murakami, and A. Matsuzawa, "A 0.114-mW dual-conduction class-C CMOS VCO with 0.2-V power supply," *IEEE symp. VLSI Circuits(VLSIC)*, pp. 228-229, Jun. 2009.

[6] Y. Takeuchi, K. Okada, and A. Matsuzawa, “An Improved Dual-Conduction Class-C VCO Using a Tail Resistor,” *IEEE MTT-S European Microwave Conference (EuMC)*, pp. 204-207, Oct. 2011.

[7] L. Fanori, A. Liscidini, and P. Andreani, “A 6.7-to-9.12GHz 55nm CMOS Hybrid Class-B/Class-C Cellular TX VCO,” *IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers,* pp.354-356, Feb. 2012.

[8] W. Deng, K. Okada, and A. Matsuzawa, "A feedback class-C VCO with robust startup condition over PVT variations and enhanced oscillation swing," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 499-502, Sep. 2011.

[9] W. Deng, K. Okada, and A. Matsuzawa, “Class-C VCO With Amplitude Feedback Loop for Robust Start-Up and Enhanced Oscillation Swing,” *IEEE Journal of Solid-State Circuits*,vol.48,no.2, pp.429-440,Feb. 2013.

[10] J. Chen, F. Jonsson, M. Carlsson, C. Hedenes, and L.R. Zheng, “A low power, start-up ensured and constant amplitude class-C VCO in 0.18 µm CMOS,” *IEEE Microwave Wireless Component Letter*, vol. 21, no. 8, pp. 427-429, Aug. 2011.

[11] M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, “High-swing class-C VCO,” *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 495-498, Sep. 2011.

[12] L. Fanori, and P. Andreani, “Low-phase-noise 3.4-4.5 GHz dynamic-bias class-C CMOS VCOs with a FoM of 191 dBc/Hz,” *IEEE European Solid-State Circuits Conference (ESSCIRC)*, pp. 406-409, Sep. 2012.

[13] H.H. Hsieh and L.H. Lu, "A High-Performance CMOS Voltage-Controlled Oscillator for Ultra-Low-Voltage Operations," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 3, pp. 467-473, Mar. 2007.