A 0.84ps-LSB 2.47mW Time-to-Digital Converter Using Charge Pump and SAR-ADC

Zule Xu, Seungjong Lee, Masaya Miyahara, and Akira Matsuzawa

Tokyo Institute of Technology, Japan

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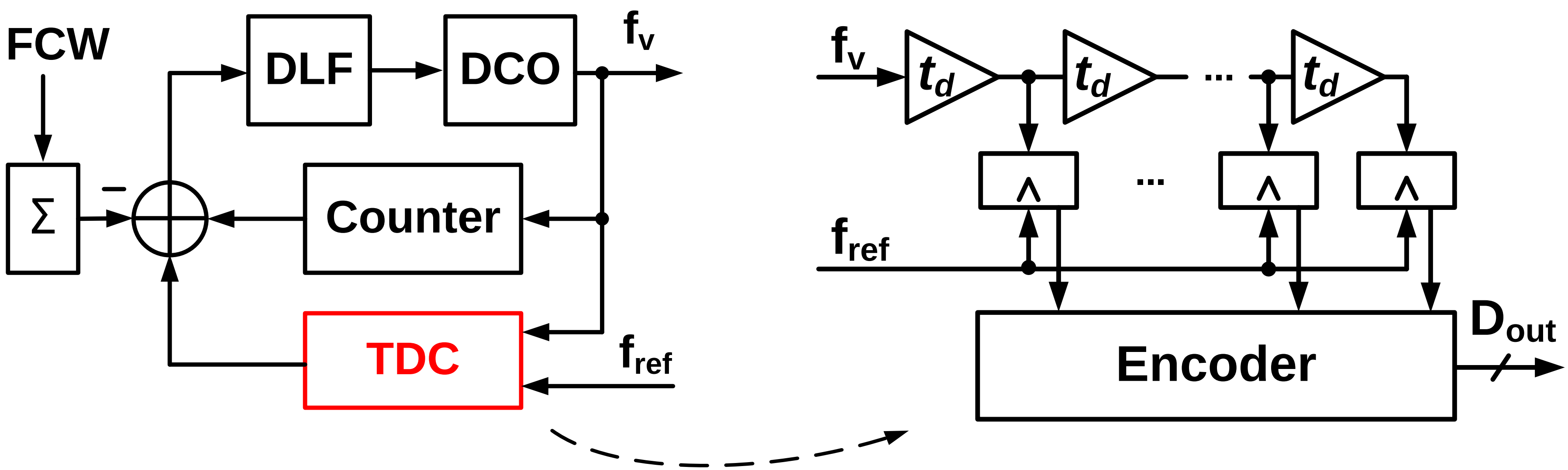
Outline

- **Motivation**
- **Issues of conventional techniques**
- **Proposed TDC**
- **Measured performance**
- **Conclusion**

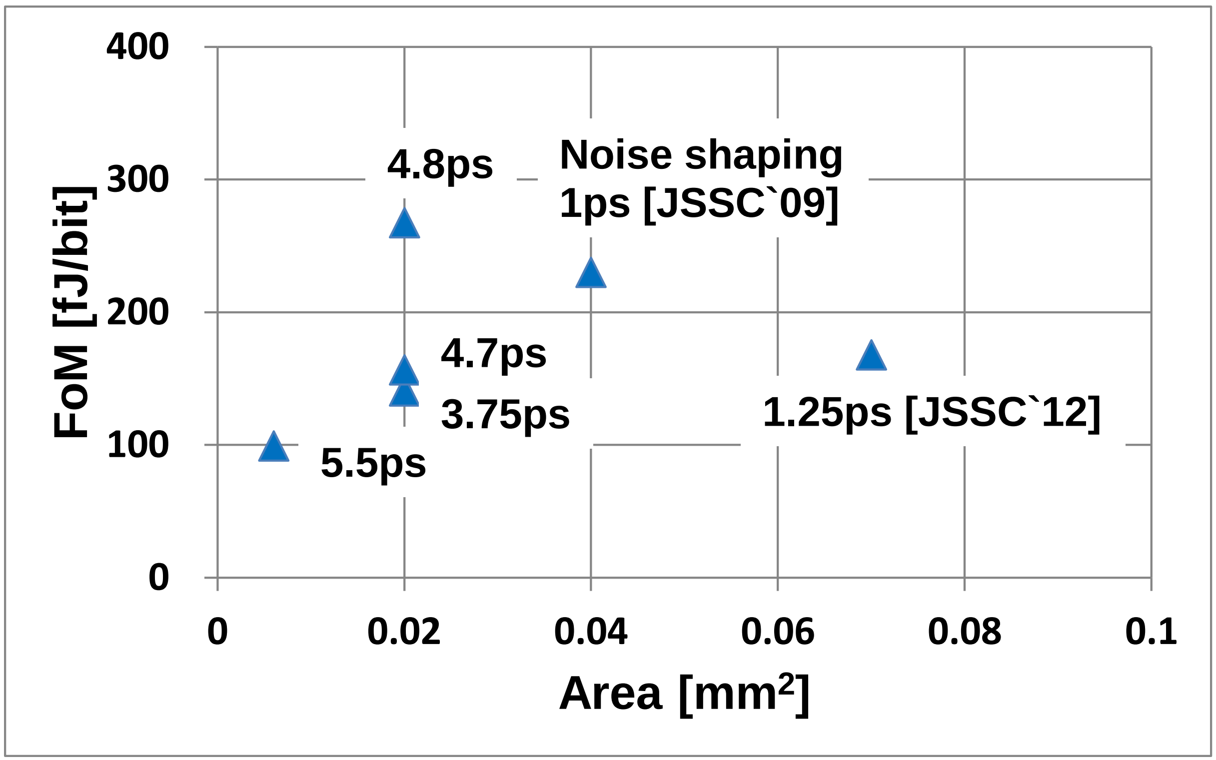
Motivation

- A fine resolution TDC contributes low in-band phase noise to a digital PLL
- Example: f_v = 4GHz, f_{ref} = 40MHz, PN = -120dBc/Hz
  → t_{res} = 0.87ps !
- Delay-chain's resolution is limited to its unit delay



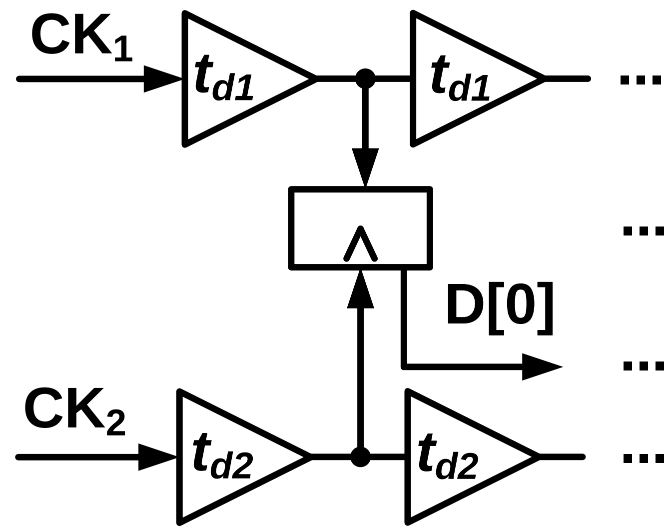
Motivation

- **For finer resolution, more <u>energy</u>, more <u>area</u>, or more <u>conversion times</u> are traded off**
- **Is there a solution for the best balance?**

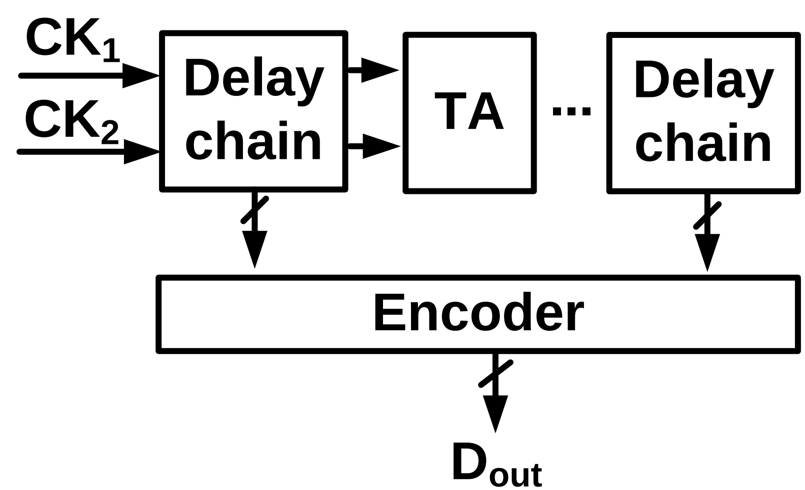


Issues of Recent Techniques

- **Vernier chain**
  - **PVT and jitter effects**
  - **Arbiter's metastability (unacceptable when the input <= 1ps)**

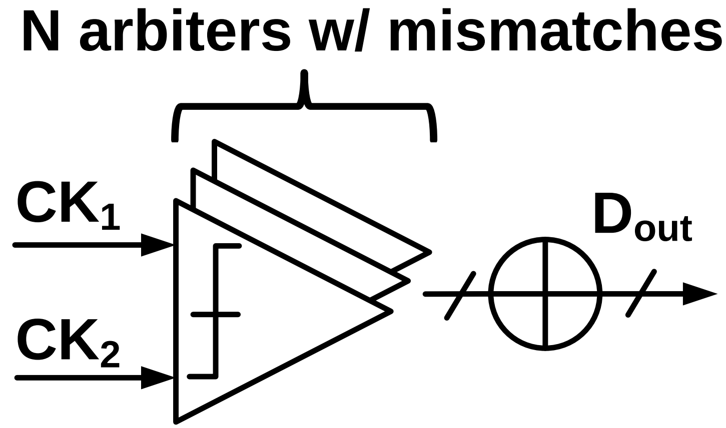


- **Pipeline**
  - **Nonlinearity of the time amplifier (TA)**
  - **Mismatch**

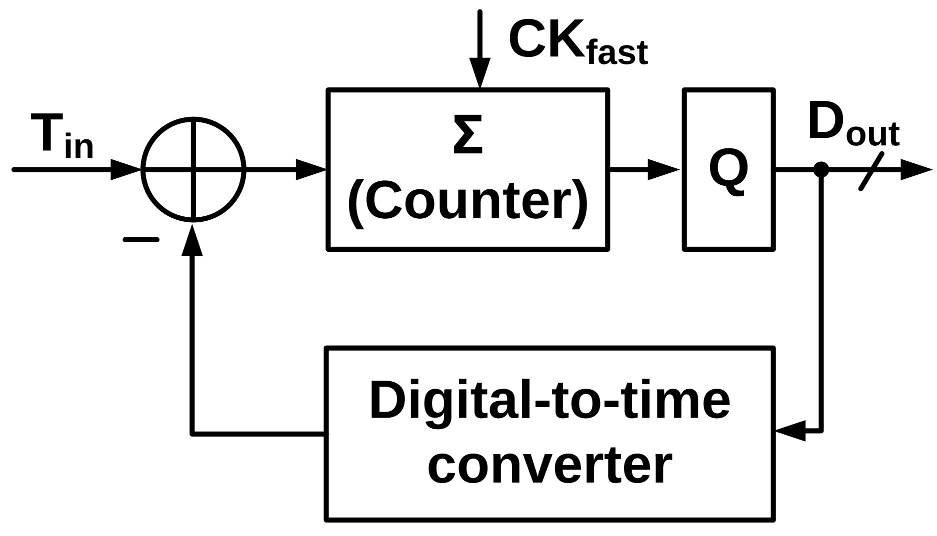


Issues of Recent Techniques

- **Stochastic**
  - **Short linear range**
  - **Highly dependent on layout and process**



- **Noise shaping**
  - **Low input signal bandwidth**
  - **Requires a fast clock for the counter**

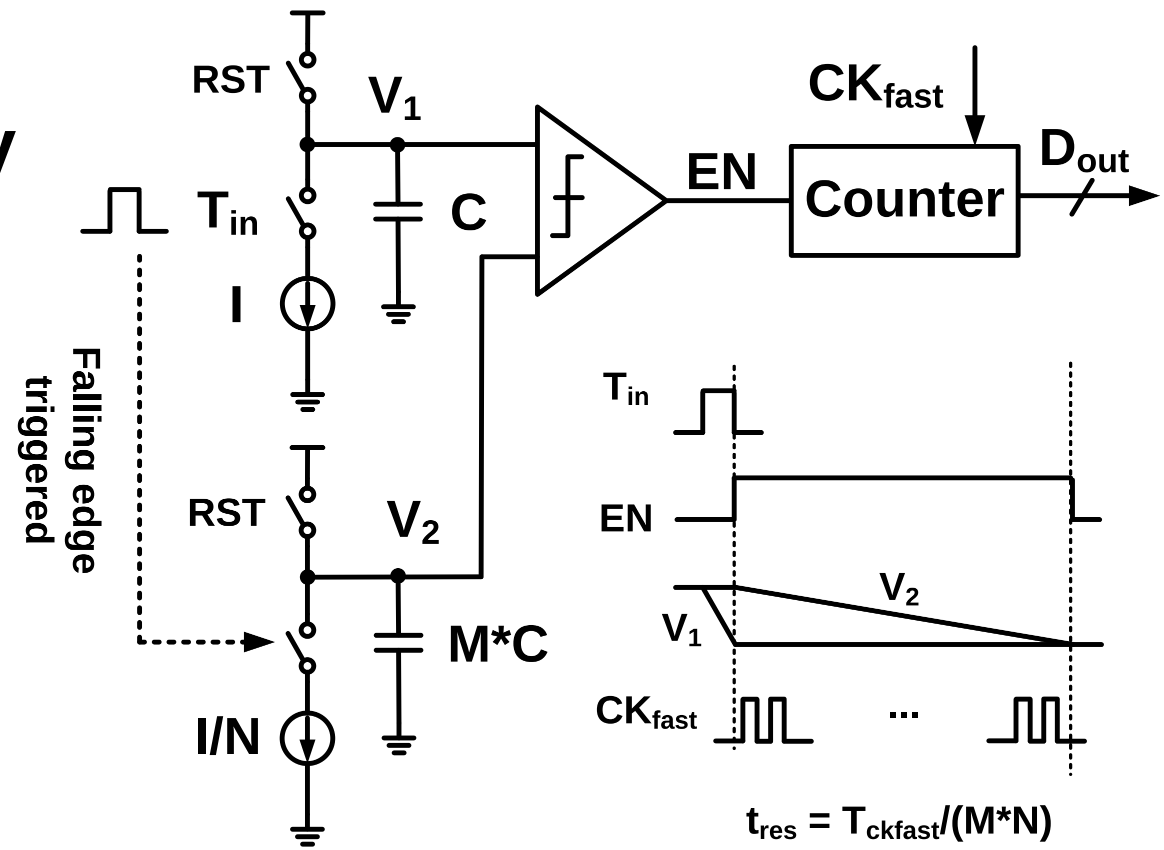


Issues of a Previous Technique

- **Time-to-amplitude conversion has achieved fine resolution but…**

- **Fast clock necessary**
- **Large capacitance**
- **Susceptible to leakage**
- **Low speed**

t_{res} = 32ps, 0.5um BiCMOS [E.R.Ruotsalainen, et.al, pp.1507-1510, JSSC 2000]

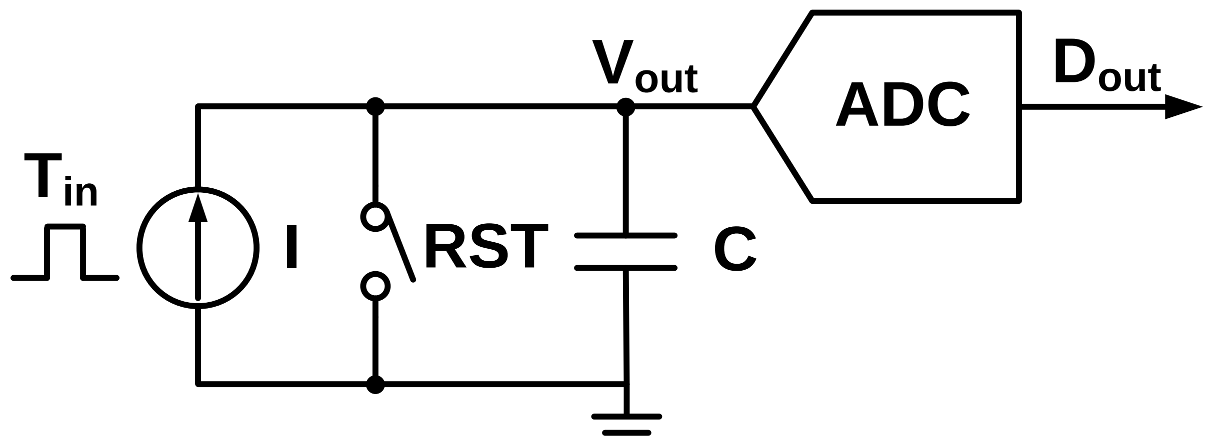


Time-to-Charge Conversion

- **Time-to-charge conversion suggests the potential for extremely fine resolution**

$$t_{res} = C*V_{lsb}/I$$

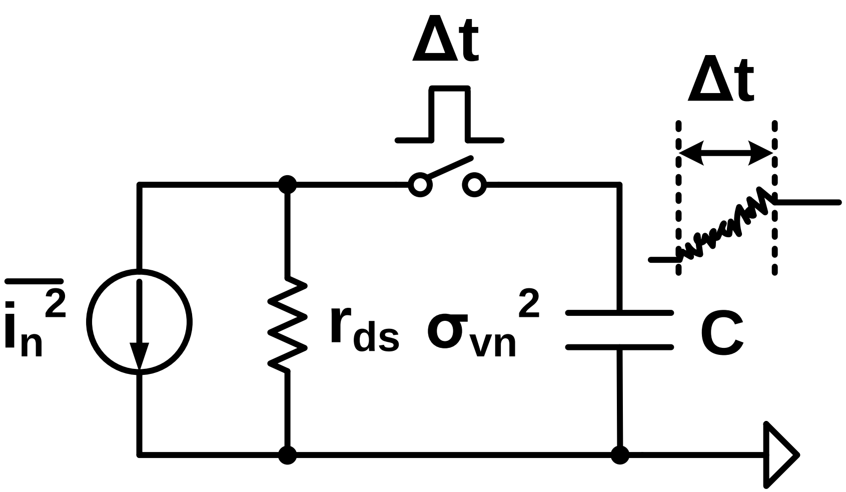
C	1pF
I	1mA
V_{lsb}	1mV
t_{res}	1ps



- **Thermal noise restricts C and I**

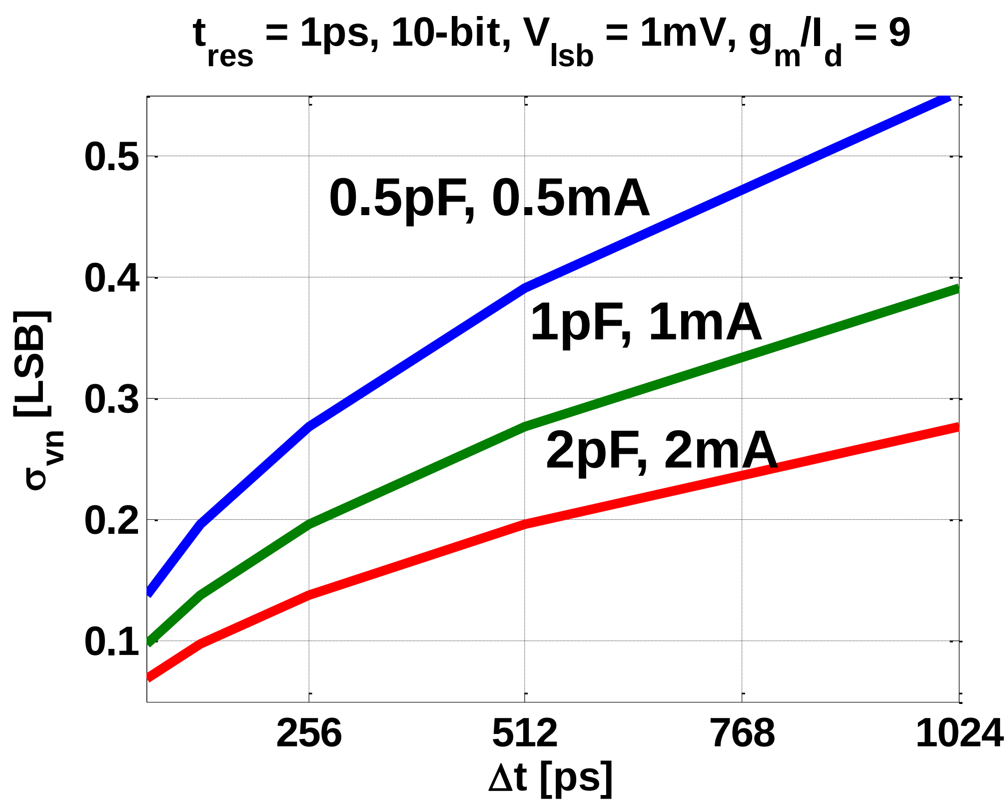
Thermal Noise

- **Noise increases with integration time (Δt)**
- **Trade-off exists between power (I) and area (C)**

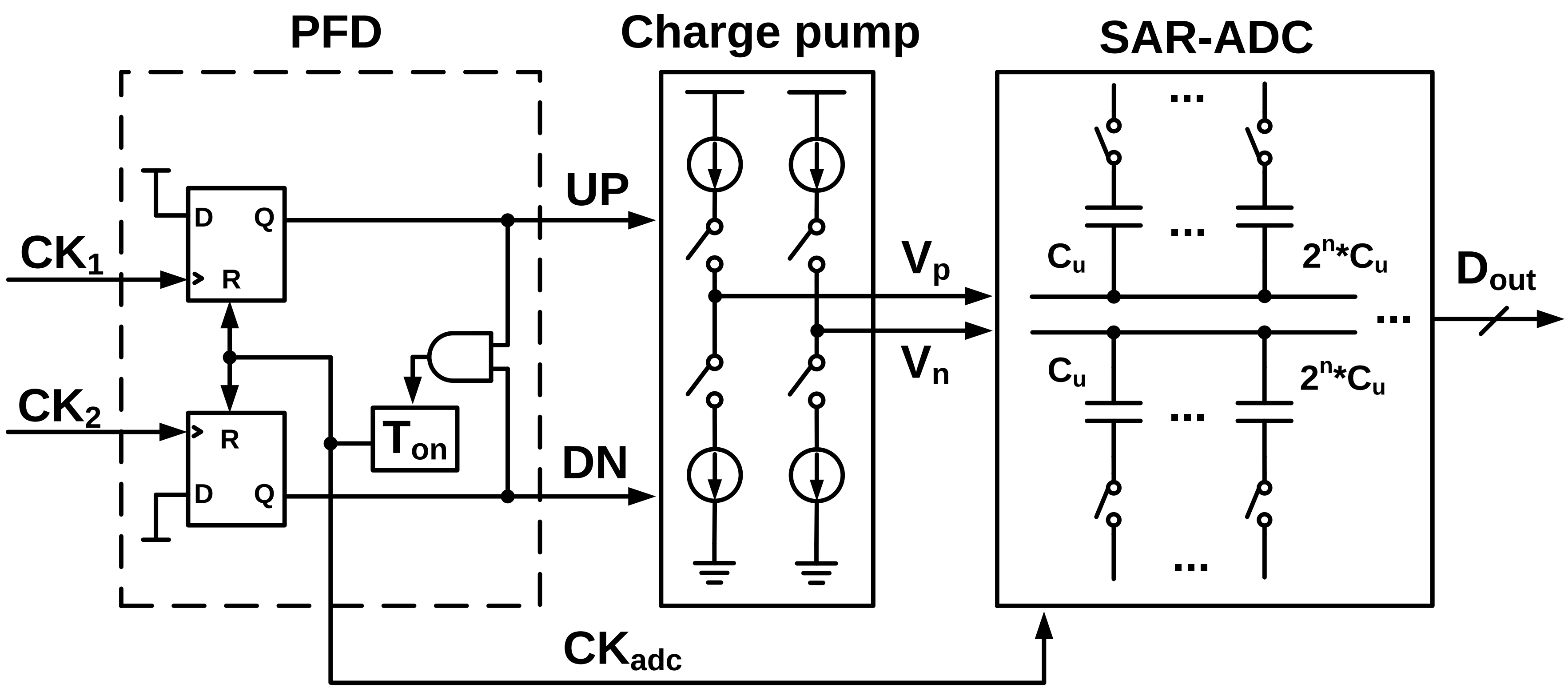


$$\sigma_{vn}^{\;2} = 4kT\gamma \cdot \frac{\Delta t}{C} \cdot \frac{V_{lsb}}{t_{res}} \cdot \boxed{\frac{g_m}{I_d}}$$

A constant for transistor sizing

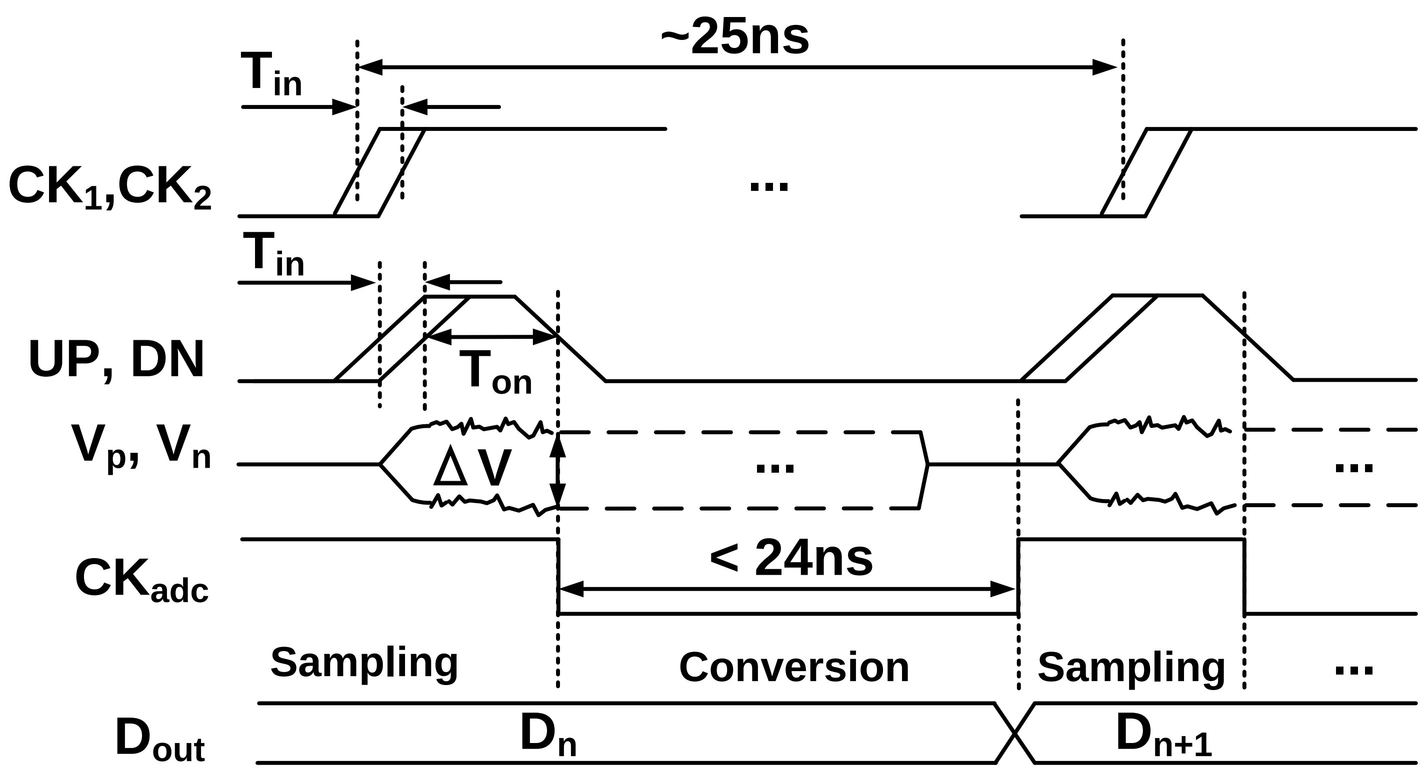


Proposal



- **Time-to-charge conversion on a SAR-ADC**
- **Short T_{on} is required to suppress the noise; $T_{on} \approx$ 200ps in this design**

Noise and Speed

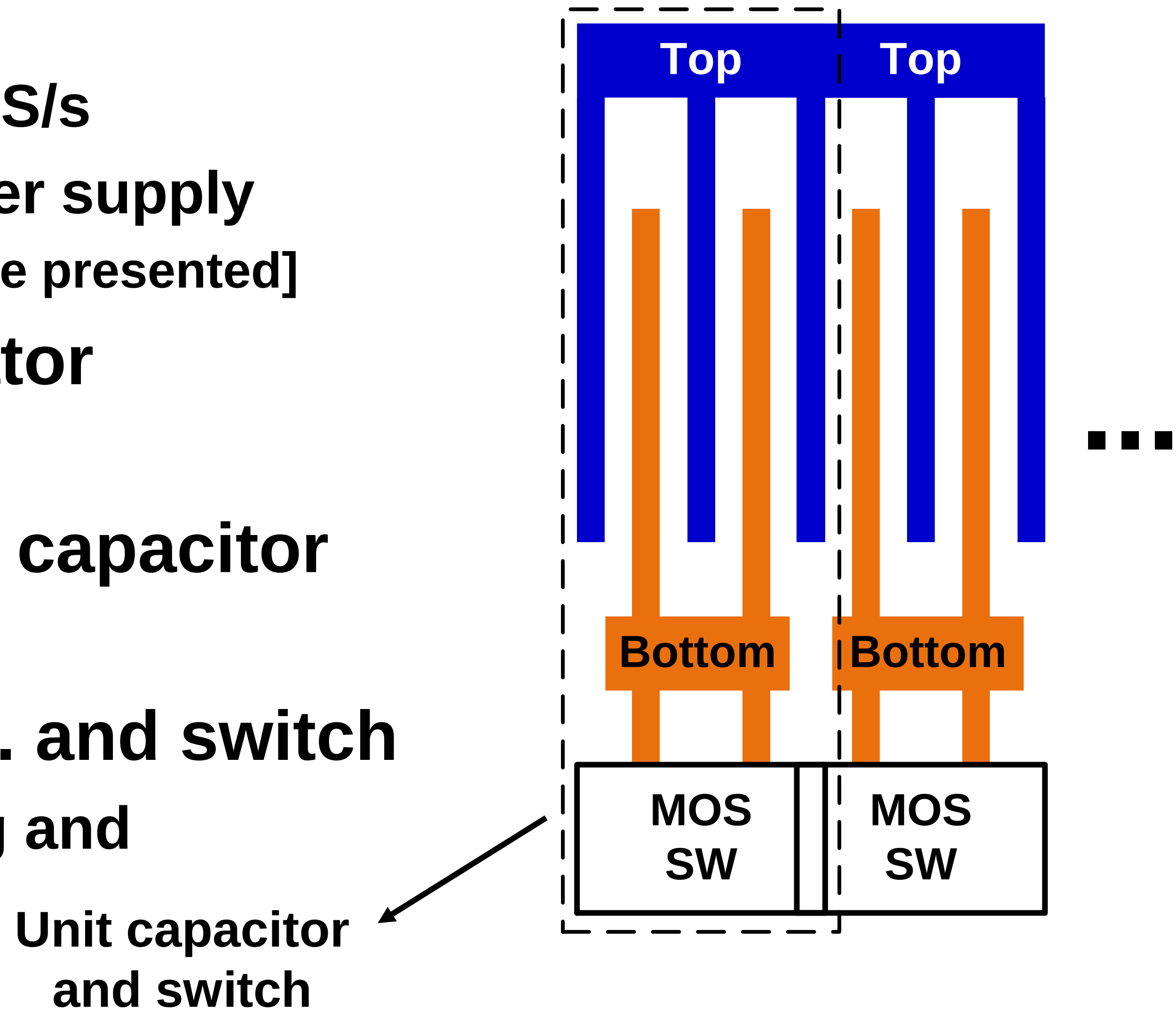


1) Thermal noise from the charge pump accumulated during (T_{in}+T_{on})
2) SAR-ADC should be faster than 40MS/s

SAR-ADC

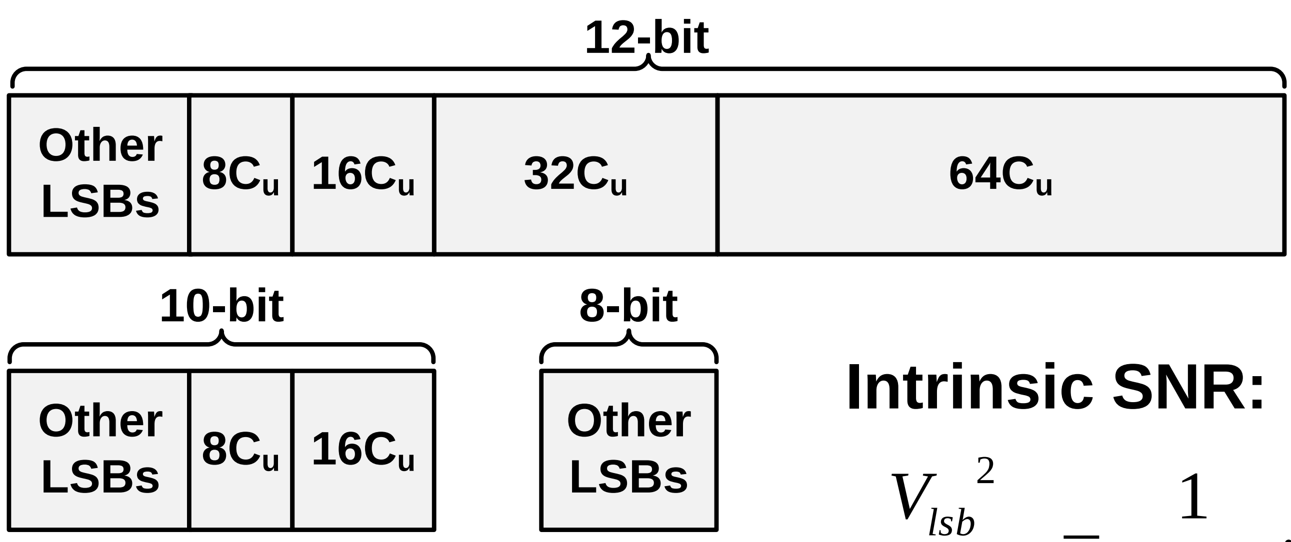
- **12-bit topology**
  - **10-bit ENOB@40MS/s**
  - **1.6mW@1.0V power supply**

  [S. Lee, SSDM 2013, to be presented]
- **Dynamic comparator**
  - **→ Low power**
- **Metal-Oxide-Metal capacitor**
  - **→ High density**
- **Same pitch of cap. and switch**
  - **→ Better matching and scalability**



Scaling of the SAR-ADC

- **Down scaling → lower power and smaller area → shorter range but not harmful for an integer-N PLL**
- **Resolution and intrinsic SNR are not degraded since the required charges are not changed**



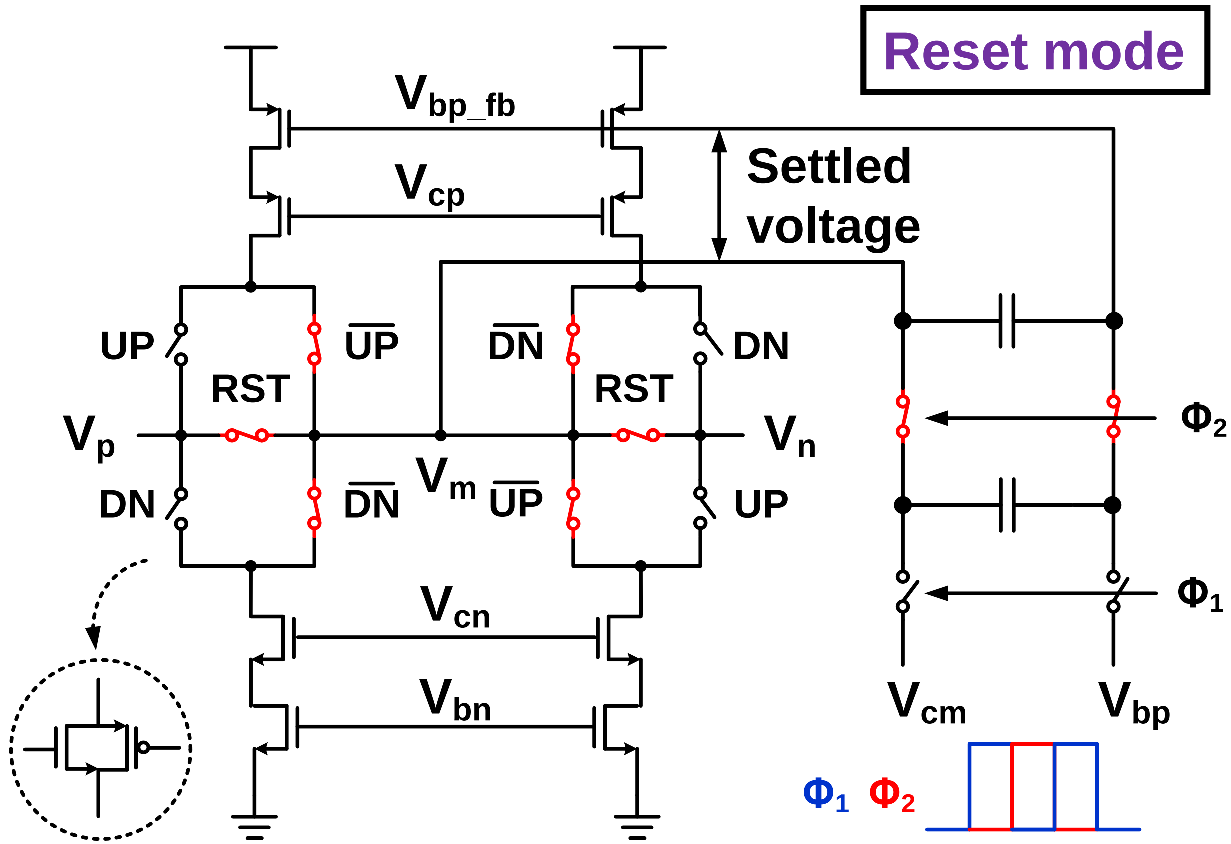
Intrinsic SNR:

Unchanged Q^2

$$\frac{V_{lsb}^{2}}{\sigma_{vn,diff}^{2}} = \frac{1}{2kT\gamma}\cdot\frac{CV_{lsb}\cdot t_{res}I_{cp}}{g_{mn}+g_{mp}}\cdot\frac{1}{T_{in}+T_{on}}$$

Charge Pump

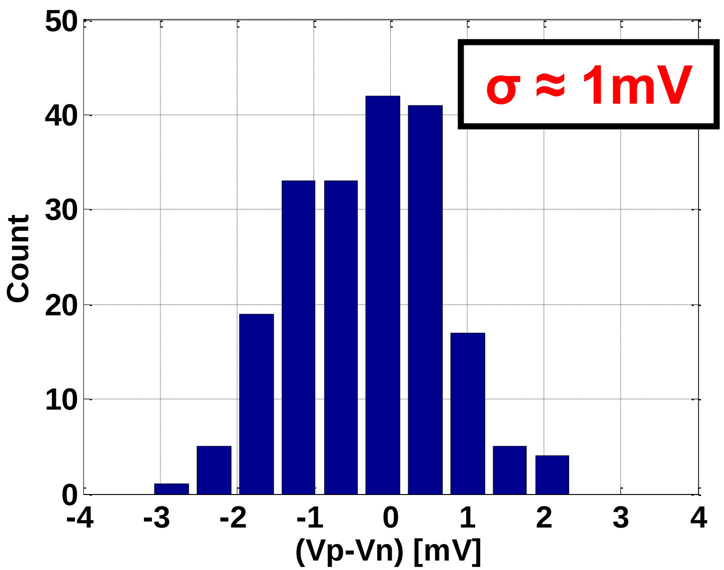
- **The CMFB matches the currents of PMOS and NMOS**
- **Conventional**
  - **Amplifier-based CMFB**
- **Proposal**
  - **Switched-capacitor CMFB**
  - **For low power and low voltage**



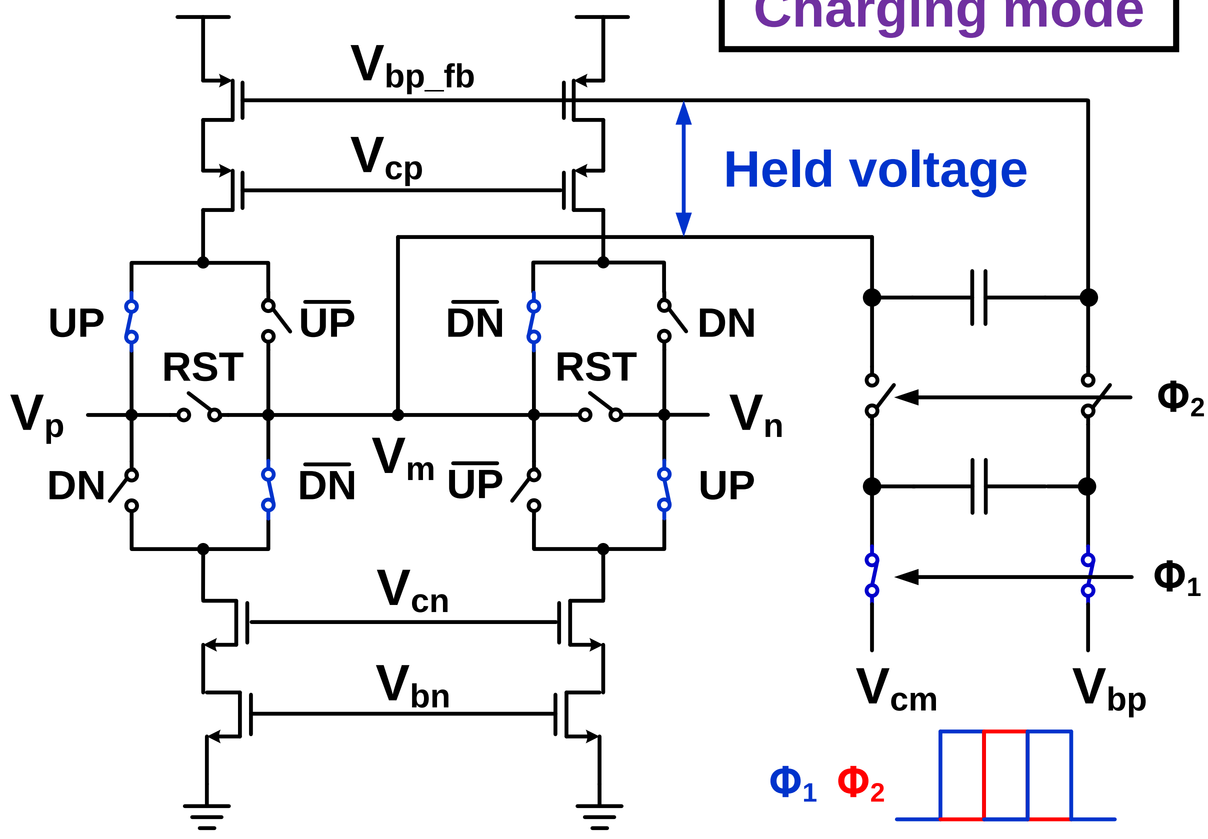
Charge Pump

- Other mismatches contribute to a static offset
- It can be canceled in the digital domain

Monte-Calo simulation
of the output voltage
(Δt=0, 1pF load cap.)

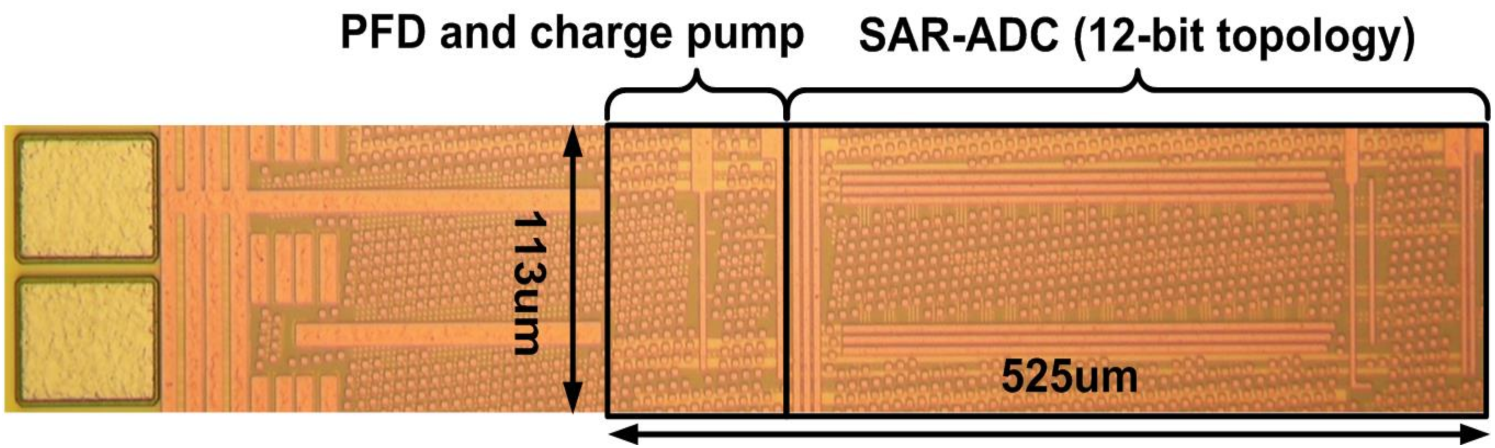


Charging mode

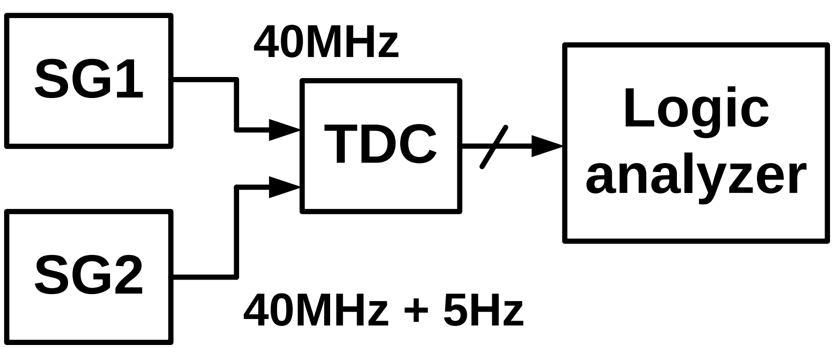


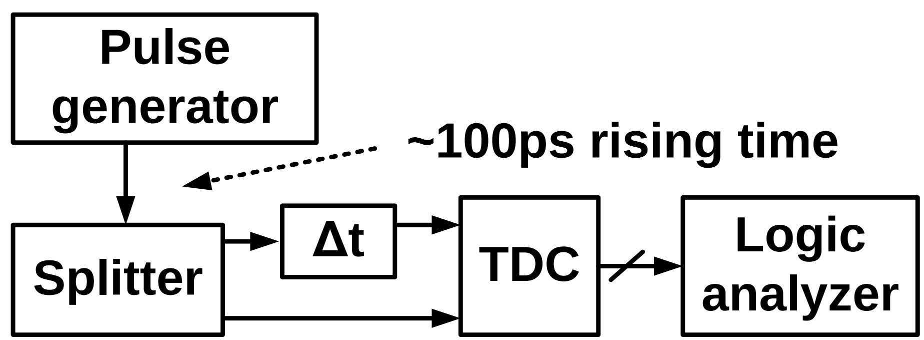
Implementation

- **CMOS 65nm, core area = 0.06mm²**



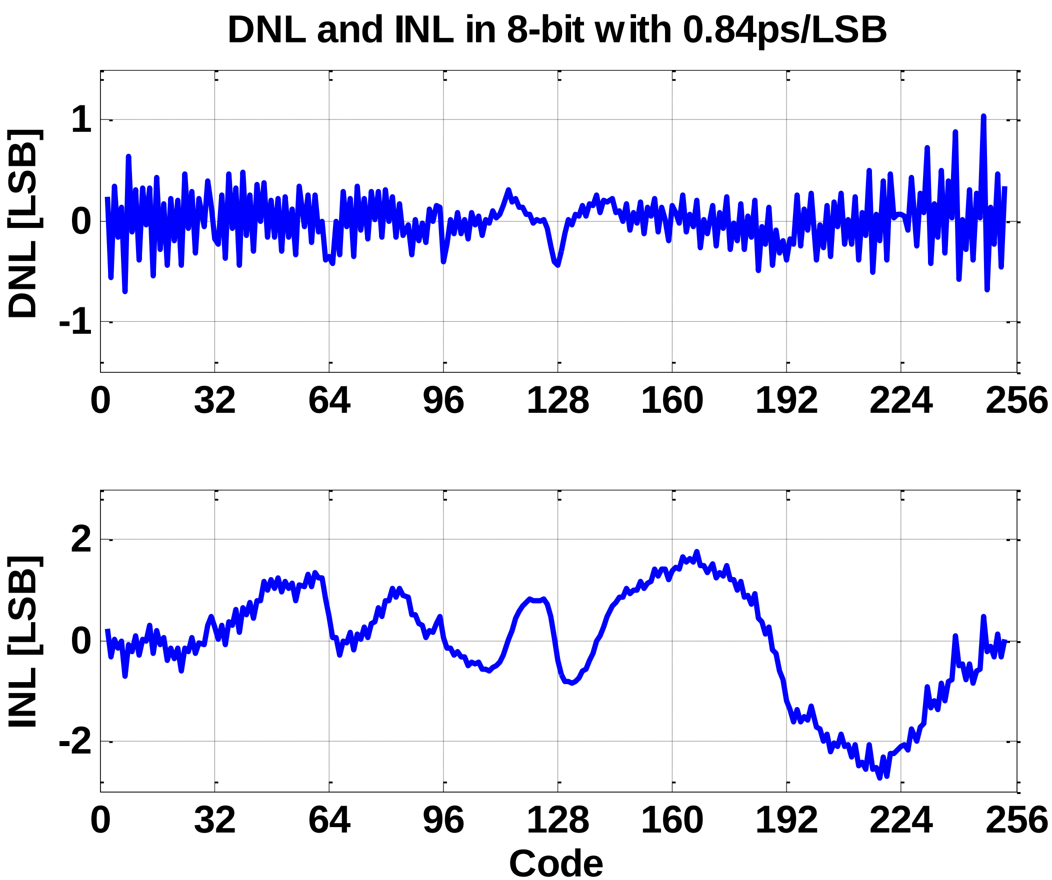
- **Measurement setups**





Measurement

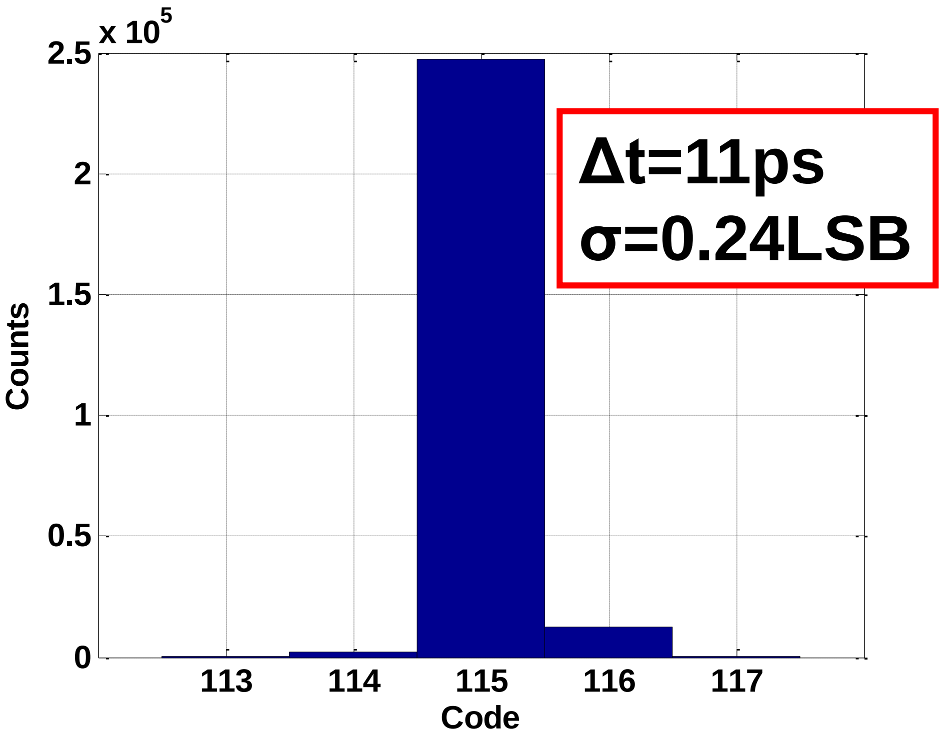
- **DNL and performance summary**

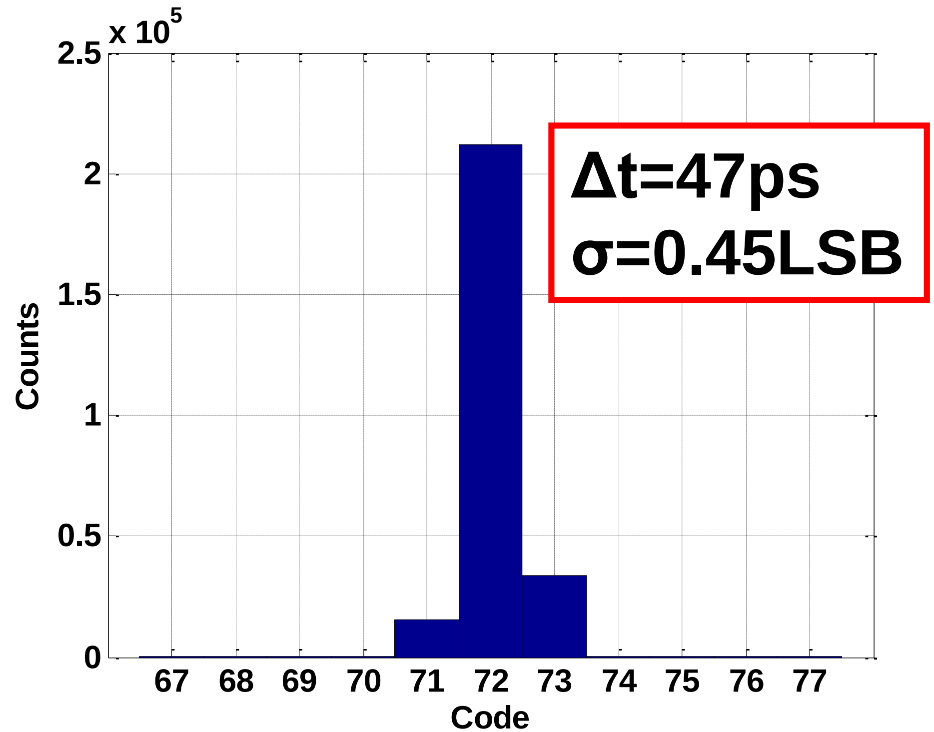


Performance	Value
CMOS [nm]	65
Supply [V]	1.0
Conv. Rate [MS/s]	40
Power [mW]	2.47
Resolution [ps]	0.84
Range [bits]	8
DNL [LSB]	-0.7/1.0
INL [LSB]	-2.7/1.7

Measurement

- **Single-shot precision: < 1LSB**
- **The thermal noise increases with longer input time interval**





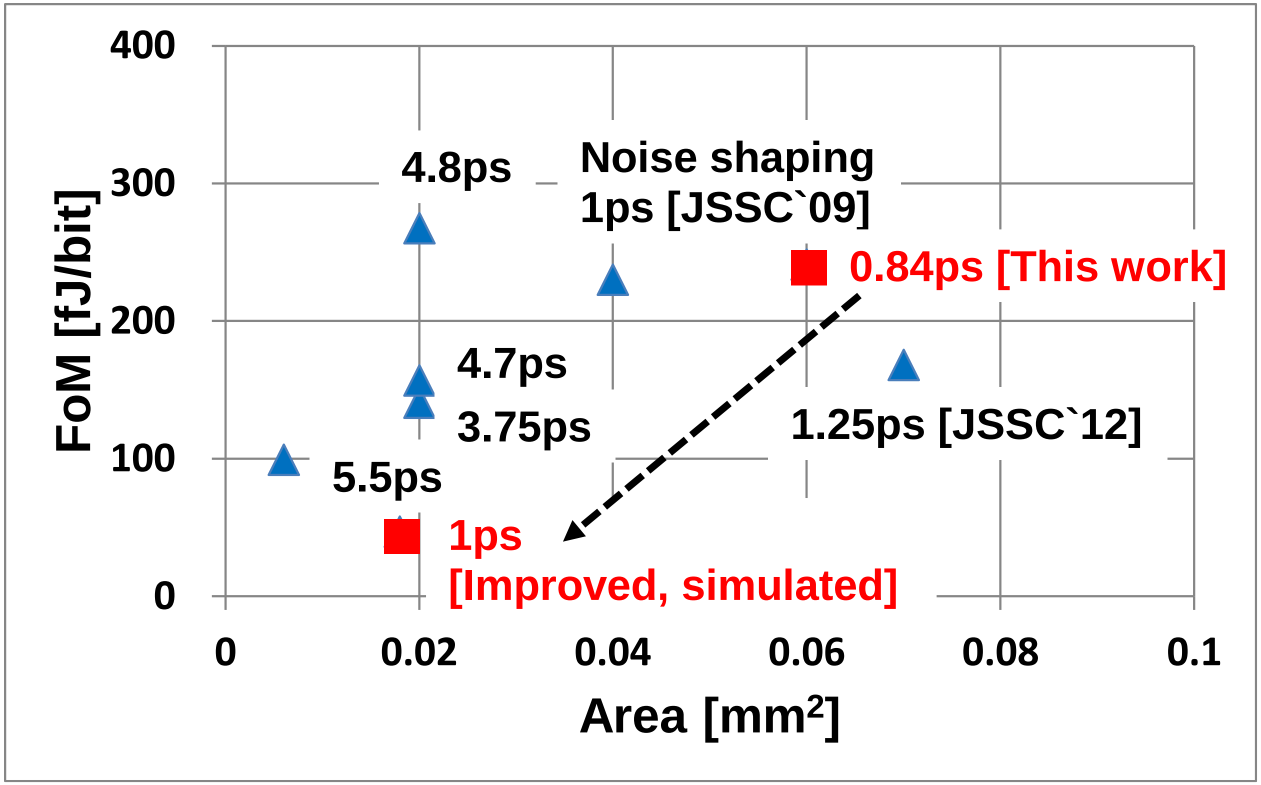
Performance Comparison

- **Best balance is achieved**

	JSSC'10	VLSI'11	VLSI'12	ESSIRC'10	This work	Improved (Simulated)
Type	Vernier	Pipeline	Noise Shaping	Stochastic	Charge	Charge
CMOS [nm]	65	130	130	65	65	65
Supply [V]	1.2	1.3	1.2	1.2	1.0	1.2
Resolution [ps]	4.8	0.63	3	3	**0.84**	**1**
Range [bits]	7	11	11	4	8	10
DNL [LSB]	<1	0.5	N/A	1.4	-0.7/1.0	-0.2/0.2
INL [LSB]	3.3	2	N/A	1.5	-2.7/1.7	-2.7
Frequency [MHz]	50	65	90 (OSR:16)	40	40	100
Power [mW]	1.7	10.5	3.2	8	**2.47**	**4**
Area [mm²]	0.02	0.32	0.43	0.04	**0.06**	**0.018**

Energy and Area Efficiencies

- **Best balance is achieved**



Energy efficiency:

$FoM = Power / Frequency / 2^N$ **or** $FoM = Power / 2 / BW / 2^N$

Conclusion

- **The proposed TDC has achieved 0.84ps resolution, 2.47mW power consumption, and 0.06mm^2 area**
- **The proposed TDC suggests the best balance among resolution, energy, area, and conversion times**
- **The proposed TDC has no issues from delay chains, TAs, or arbiters**
- **The proposed TDC can be a practical solution for digital PLLs**

Acknowledgement

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Thank you for your interest!

Zule Xu,
xuzule@ssc.pe.titech.ac.jp