A Full 4-Channel 60 GHz Direct-Conversion Transceiver

Seitaro Kawai, Ryo Minami, Ahmed Musa, Takahiro Sato, Ning Li, Tatsuya Yamaguchi, Yasuaki Takeuchi, Yuki Tsukui, Kenichi Okada, and Akira Matsuzawa Dept. Physical Electronics, Tokyo Institute of Technology Tel: +81-3-5734-3764, Fax: +81-3-5734-3764, E-mail: kawai@ssc.pe.titech.ac.jp

Abstract— This paper presents a 60-GHz direct-conversion transceiver in 65 nm CMOS technology. By the proposed gain peaking technique, this transceiver realizes good gain flatness and is capable of more than 7 Gbps in 16QAM wireless communication for all channels of IEEE802.11ad standard within EVM of around -23 dB. The transceiver consumes 319 mW in transmitting and 223 mW in receiving, including the PLL consumption.

I. Introduction

Recently, wireless communications in mm-Wave, especially in 60-GHz are expected because the frequency bands around 60-GHz are available without any license in many countries. The IEEE802.11ad standard defines four 2.16-GHz bandwidth channels in 57.24GHz to 65.88GHz and it is capable of achieving 7 Gbps for 16QAM by each channel. To realize 16QAM communication, EVM is a very important factor, which is associated with phase noise, I/Q mismatch, LO leakage and gain flatness. Table I shows the relationship between gain flatness and EVM, without considering other factors. EVM has to be less than -17 dB to communicate with 16QAM, so the gain flatness has to be kept below 2 dB. Gain flatness can be improved by equalizing in baseband, but in a high speed communication system, it consumes a lot of power. This work improves gain flatness by the proposed gain peaking technique and realizes communication for 16QAM in all channels.

II. PROPOSED TRANSCEIVER

Fig. 1 shows the block diagram of the proposed transceiver, using a 65 nm CMOS process. The transmitter consists of a 4-stage PA, differential preamplifiers, I/Q double-balanced Gilbert mixers and a quadrature injection-locked oscillator(QILO). The matching block uses $6\,\mu$ m-width transmission line to reduce area. In addition, the capacitive-cross-coupling technique is used to improve gain and I/Q isolation. The receiver consists of a 4-stage LNA, differential amplifiers, I/Q passive mixers, a QILO, and a baseband LNA. The LNA employs common-source common-source topology to improve the noise figure.

Fig. 2 shows the baseband amplifier employing gain equalizing technique, and Fig. 3 shows the gain and NF compared to the previous work [2]. In the previous work, the gain deteriorates in high frequency, and it influences on the total gain flatness of the receiver. In this work, the common-source amplifier is employed in input to compensate for gain. The gain is equalized in 1-GHz to 2-GHz, and a good flatness is achieved. In addition, NF is around 2 dB in large bandwidth.

III. MEASUREMENT RESULTS AND CONCLUSION

Fig. 4 shows a die photo of the chip using a standard 65 nm CMOS technology. The chip size is $4.2 \, \text{mm} \times 4.2 \, \text{mm}$. The antenna built in a package is used, and it has a 6-dBi gain. The transmitter and receiver consume 257 mW and 162 mW from

a $1.2\,\mathrm{V}$ supply, respectively. The PLL consumes 61 mW from the $1.2\,\mathrm{V}$ supply.

Fig. 5(a) shows the measured Rx conversion gain. Rx has a low-gain mode and a high-gain mode to avoid saturating signal. These two modes are adjustable by changing bias voltage of the LNA. Moreover, the conversion gain achieves good flatness, suppressed under 1 dB for every channel because of the gain peaking technique of the BB amplifier. Fig. 5(b) shows the measured power characteristics, NF and the signal to noise and distortion ratio (SNDR) derived from IM3 and NF. IIP3 of Rx is -14 dBm in low-gain mode.

Table II shows the measurement results for 16QAM, showing the constellation, spectrum, back-off, RF data rate, EVM, SNR(MER) and communication distance. The symbol rate is 1.76 Gs/s with a roll-off factor of 25 %, and the RF data rate with 2.16-GHz bandwidth are 7.04 Gbps for 16QAM. The maximum data rate measured in a wider bandwidth for 16QAM with a 25 % roll-off is 10 Gbps within a BER of 10⁻³. The measured EVM is around -23 dB in every channel, which is normalized by the maximum symbol amplitude.

Table III shows a performance comparison with other 60-GHz transceivers. The proposed transceiver integrates Tx, Rx, LO including PLL, and is evaluated with the embedded antennas. This front-end covers all four channels of 60-GHz and achieves full-data rates for QPSK and 16QAM with the best EVM.

IV. Conclusion

The 60-GHz direct-conversion transceiver can communicate with 16QAM in every channel of IEEE802.11ad standard. The gain flatness is improved by the proposed gain peaking technique, which contributes to good EVM of around -23 dB.

Acknowledgements

This work was partially supported by MIC, MEXT, STARC, NEDO, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

References

- [1] K. Okada, *et al.*, "A full 4-channel 6.3Gb/s 60GHz direct-conversion transceiver with low-power analog and digital baseband circuitry," in ISSCC Dig. Tech. Papers, pp. 218-220, Feb. 2012.
- [2] K. Okada, et al., "A 60GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE 802.15.3c," in ISSCC Dig. Tech. Papers, pp. 160-162, Feb. 2011.
- [3] H. Asada, et al., "A 60GHz 16Gb/s 16QAM low-power direct-conversion transceiver using capacitive cross-coupling neutralization in 65 nm CMOS" in A-SSCC, pp. 373-376, Nov. 2011.
- [4] S.Emami, et al., "A 60GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," in ISSCC Dig. Tech. Papers, pp. 164-166, Feb. 2011.
- [5] V. Vidojkovic, et al., "A low-power 57-to-66GHz transceiver in 40nm LP CMOS with -17dB EVM at 7Gb/s," in ISSCC Dig. Tech. Papers, pp. 268-270, Feb. 2012.

TABLE I
GAIN FLATNESS TO EVM CORRESPONDENCE

Gain Flatness	0dB		1dB			2dB					
EVM				-22dB			-18dB				
	·		-	#	ø	*	٠	學	瘀	杂	撕
Constellation	ŀ	•			16	#	*	磐	4	4	*
Constellation	ŀ			۰	•	#	٠	*	*	旅	斞
	Ŀ		۰		-	*		藥	織	9k	躯

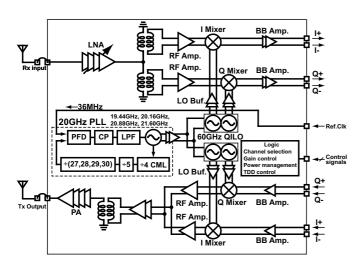


Fig. 1. Block diagram of the 60-GHz direct-conversion transceiver.

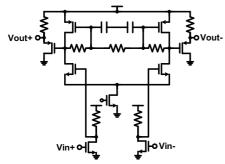


Fig. 2. Gain equalizing LNA.

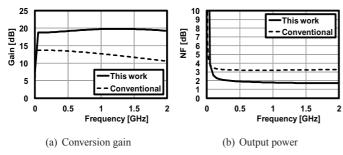


Fig. 3. Gain and NF of gain equalizing LNA.

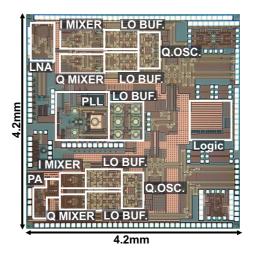


Fig. 4. Die micrograph of RF chip.

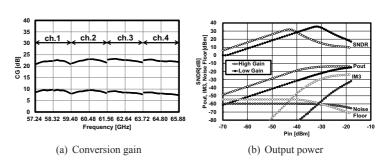


Fig. 5. Rx conversion gain and output power.

TABLE II
Measurement summary of RF-frontend for 16QAM.

Channel	ch. 1	ch. 2	ch. 3	ch. 4	Max rate
Constellation	***	() () () () () () () () () () () () () (5. 6. 6. 6. 6. 6. 6. 6. 6. 6. 6. 6. 6. 6.	2 2 2 3 4 2 3 4 4 4 2 4 4 4 4 5 4 4 5 6 7 4	48 5 4 2 4 6 2 2 4 4 4 3 4 4 5
Spectrum	7		5		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Back-off	4.4 dB	4.6 dB	5.0 dB	5.7 dB	5.0 dB (ch.3)
Data rate	7.0 Gb/s	7.0 Gb/s	7.0 Gb/s	7.0 Gb/s	10.0 Gb/s (ch.3)
EVM	-23.0 dB	-23.0 dB	-23.3 dB	-22.8 dB	-23.0 dB (ch.3)
SNR	20.4 dB	20.5 dB	20.7 dB	20.3 dB	20.4 dB (ch.3)
Distance	0.3 m	0.5 m	0.5 m	0.3 m	>0.01 m (ch.3)

TABLE III
PERFORMANCE COMPARISON

FERFORMANCE COMPARISON.						
	Max rate	Distance for BER < 10 ⁻³	P _{DC} (Tx/Rx)			
Tokyo Tech	11 Gbps [2] 16 Gbps [3]	ch.1-2 (EVM < -17 dB) 2.7 m (BPSK/QPSK) 0.2 m (8PSK/16QAM)	252 mW / 172 mW			
SiBeam [4]	7 Gbps	ch.2-3(EVM < -19 dB) 50 m (LOS) 16 m (NLOS)	1820 mW / 1250 mW			
IMEC [5]	7 Gbps	ch.1-4 (EVM < -17 dB) (not wireless)	176 mW / 112 mW			
This work	10 Gbps	ch.1-4 (EVM < -23 dB) 1.3 m-1.6 m (QPSK) 0.3 m-0.5 m (16OAM)	319 mW / 223 mW			