60 GHz カスコード増幅器の利得および安定性の解析

An Analysis of Cascode Structure for 60GHz Amplifier Design in 65nm CMOS

ト 慶紅

Qinghong Bu

李 寧 Ning Li 岡田 健一 Kenichi Okada 松澤 昭 Akira Matsuzawa

東京工業大学大学院理工学研究科電子物理工学専攻

Department of Physical Electronics, Tokyo Institute of Technology

# 1. Introduction

Cascode structure is widely used in analog circuits for its high gain. The good isolation between input and output of this structure is also attractive in mm-wave amplifier design. The amplifiers using cacode structure with gain boost technique have been reported recently [1-2]. Although the gain boost technique realizes high gain, the stable factor also should be considered when using the technique.

In this paper, a gain robust cascode structure which uses a transmission line (TL) at the gate of the common-gate transistor is analyzed considering the trade-off between the gain and the stable factor.

## 2. Analysis of gain robust cascode structure

The small-signal model of cascode circuit with a TL at the gate of common-gate transistor can be simplified as Fig. 1. With the use of  $L_{\text{TH}}$ , an incoming signal appears at the source terminal of common-gate transistor, a corresponding out-of-phase voltage is generated at the gate terminal. The voltage drop across the  $C_{\text{gs}}$  is boosted, leading to improved gain of the common-gate stage and also leads to the gain boost of cascode structure. [2]

However, the feedback caused by the inductance added in the gate of the common-gate transistor makes the stability of the cascode structure become worse. The tradeoff between the gain and the stability should be considered when choosing the value of inductance. Fig. 2 shows the simulation results of the maximum gain and the stability with different inductance at 60 GHz. The guided microstrip transmission line (GMSTL) in [3] is used in the simulation to realize different value of inductance. It obviously shows that, as the inductance increased, the maximum gain is increased while the stable factor is decreased.

For the analysis, two cascode-transistor TEGs are fabricated in a 65nm CMOS process. Both of them are 20-finger CS and 20-finger CG transistors (each with 2  $\mu$ m unit finger length) with 60  $\mu$ m and 100  $\mu$ m TL[3].

#### 3. Measurement results

The measurement results of the cascode TEGs are shown in Fig. 3. The maximum available gain is shown in Fig. 3(a). It is observed that the cascode structure with 100  $\mu$ m TL exhibits 12 dB MAG at 60GHz, which is much higher than the cascode structure with 60  $\mu$ m TL. Fig. 3(b) shows the measurement results of the stable factor. It

clearly shows that, the stable factor of the cacode structure with 100  $\mu m$  TL is worse than that with 60  $\mu m.$ 

### 4. Conclusion

A gain boost cascode structure which uses a TL at the gate of common-gate transistor is analyzed in this paper. The trade-off between the gain and the stability of the structure is shown both by simulation and measurement results. A reasonable value should be chosen when using this technique.

#### Acknowledgements

This work was partially supported by MIC, SCOPE, MEXT, STARC, NEDO, Canon Foundation and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

### References

- A. Niknejad, et al., *mm-Wave Silicon Technology 60GHz and* Beyond, Springer. 2007.
- [2] H. Hsieh, et al, IEEE RFIC, Jun. 2011.
- [3] K. Okada, et al, IEEE GSMM, Apr.2009.



Fig. 1. Small-signal model of cascode structure.



Fig. 2 The MSG/MAG and stable factor versus the length of TL at 60 GHz



Fig. 3. Measure results of casocde TEG. (a) MSG/MAG. (b) Stable factor.