An Improved Dual-Conduction Class-C VCO Using a Tail Resistor

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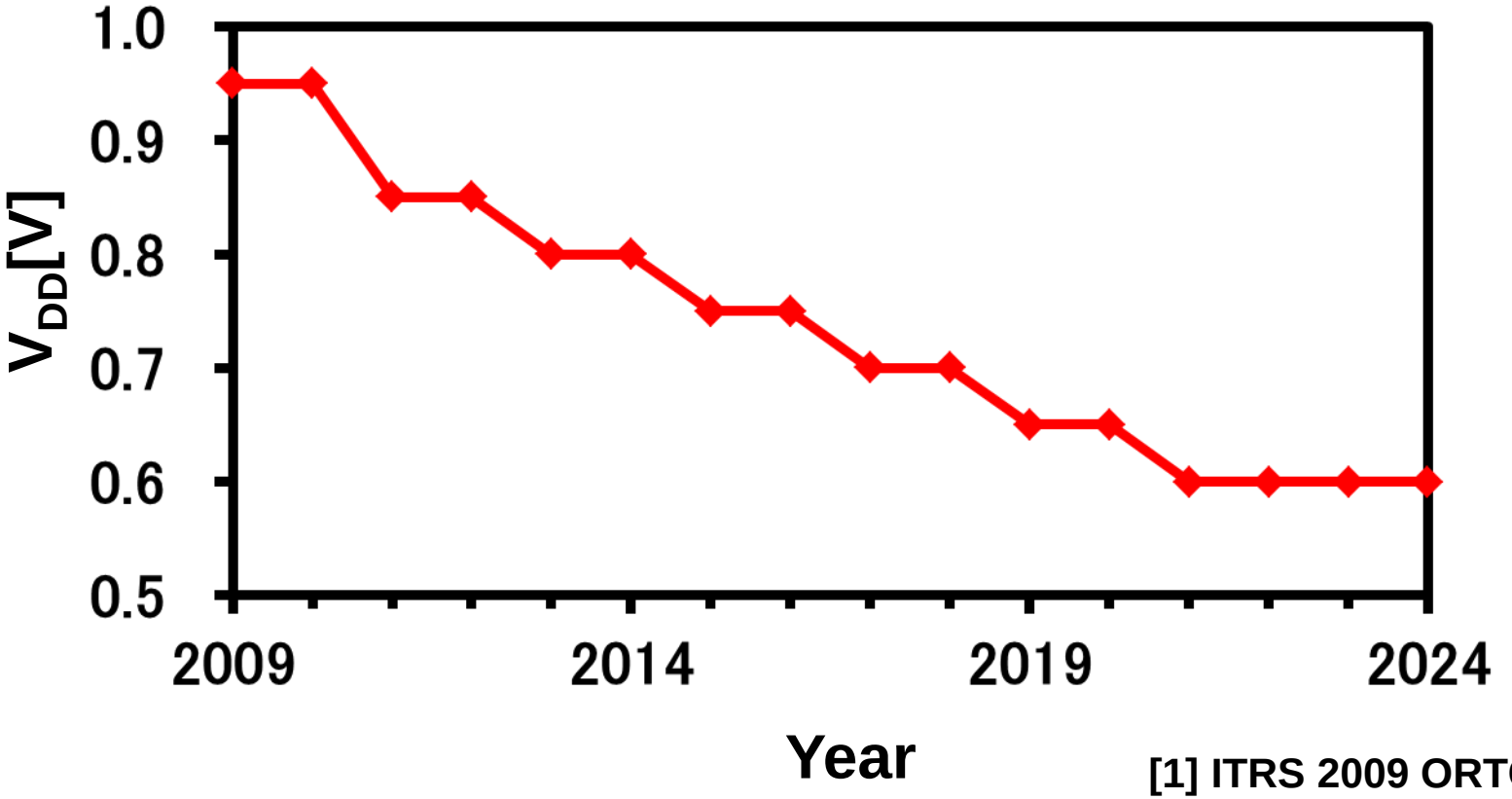
Scaling of supply voltage

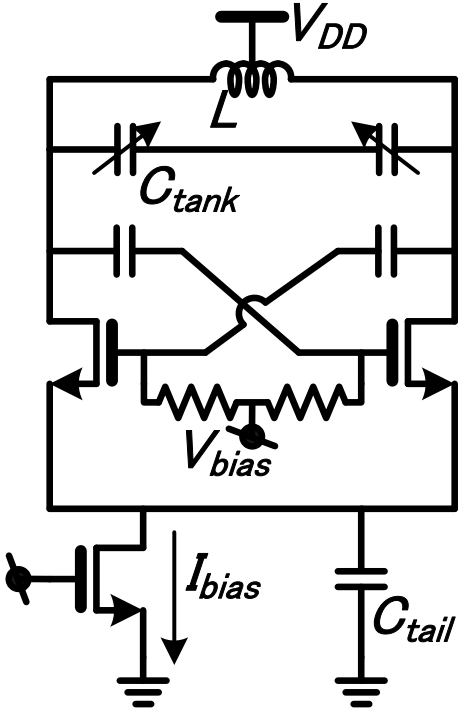


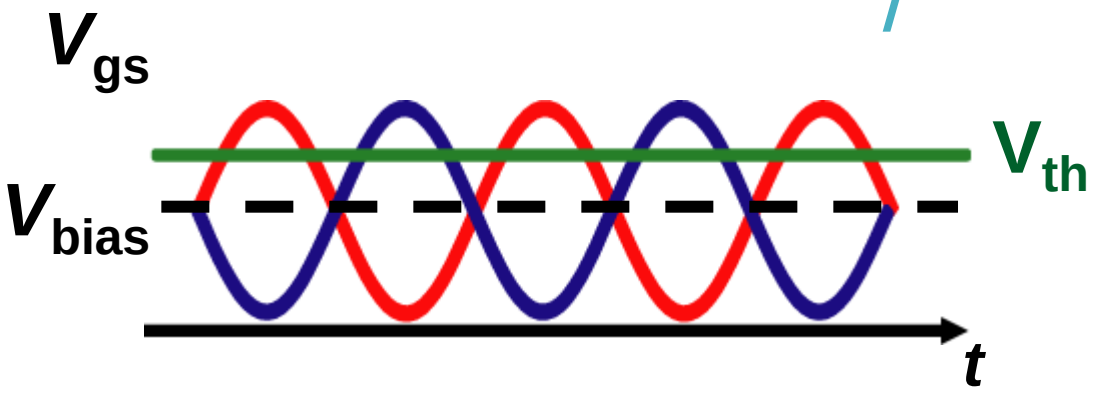
[1] ITRS 2009 ORTC

http://www.itrs.net/

Low voltage circuits are needed.

Class-C VCO[2]



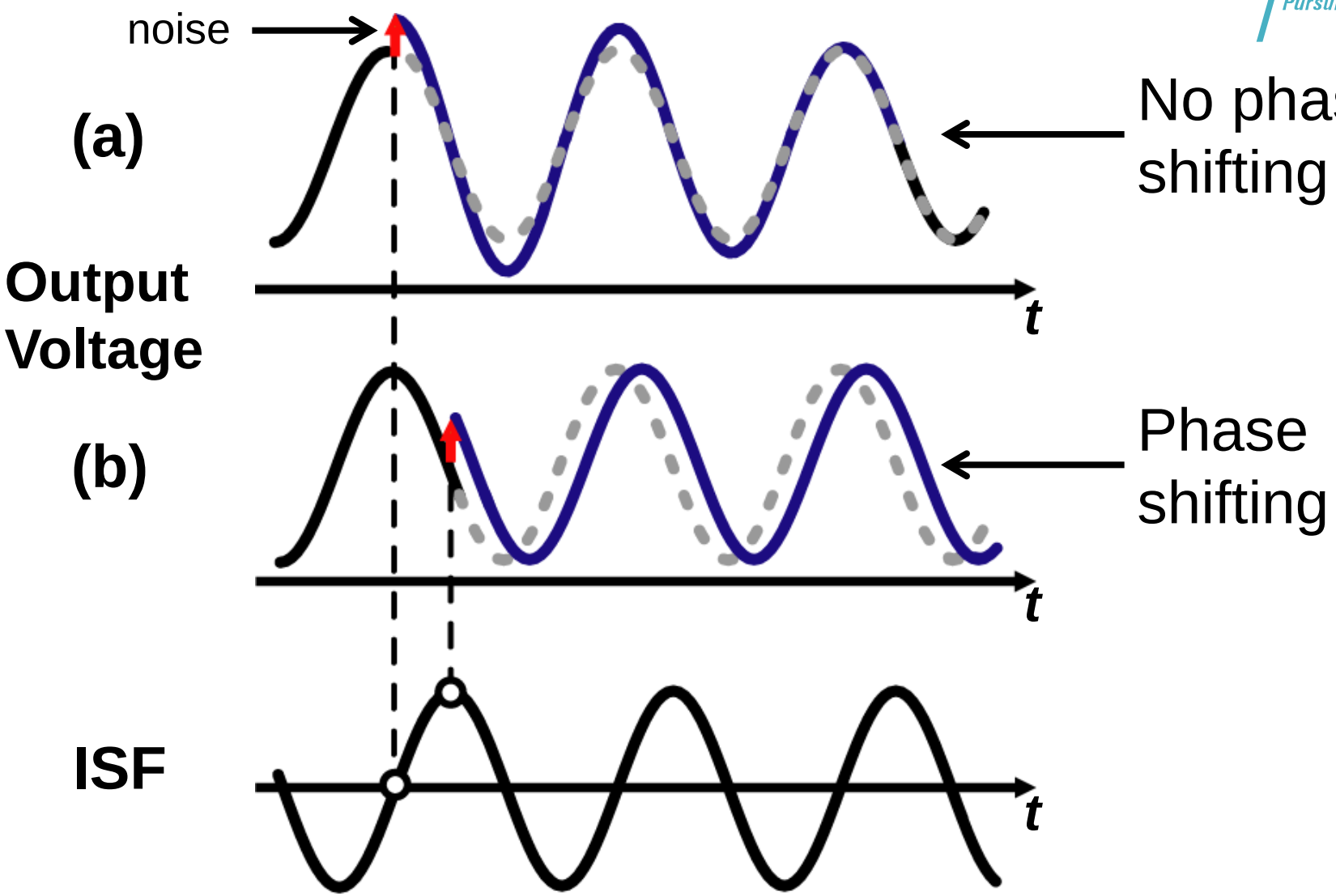


☺ It realizes low phase noise

☹ At low supply voltages, the oscillation is not robust.

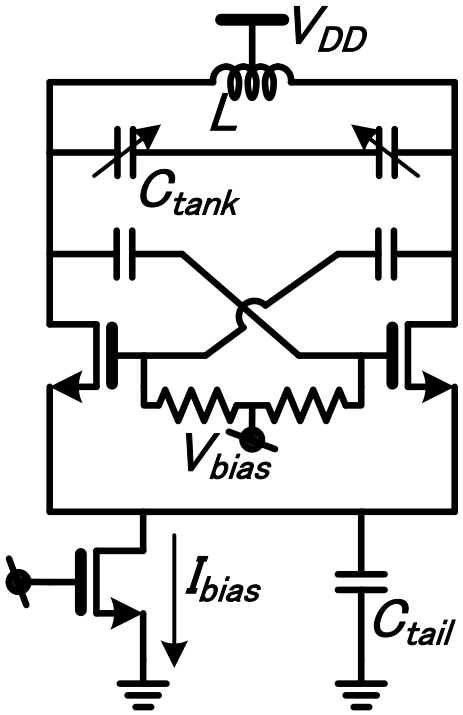
[2] A. Mazzanti, *et al*., JSSC 2008

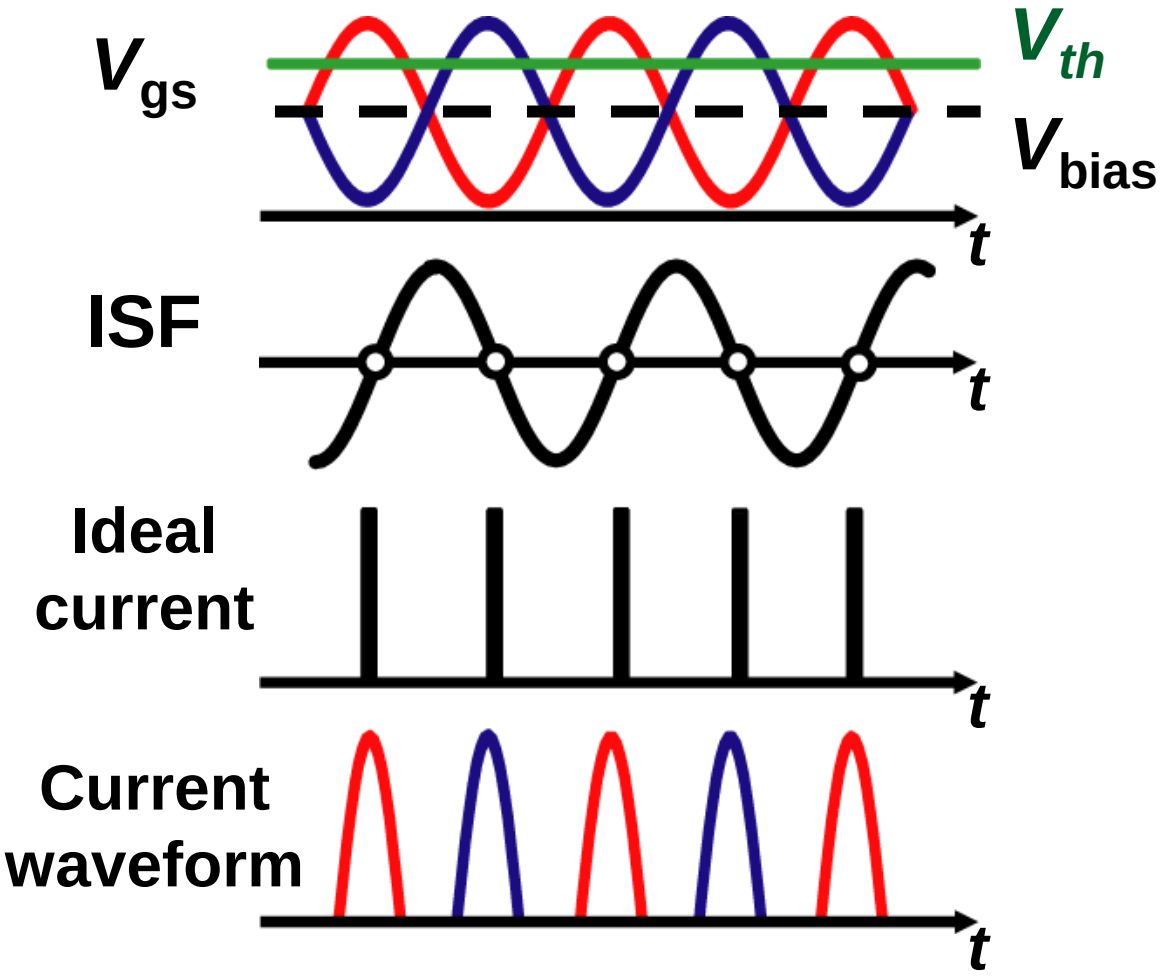
Impulse Sensitivity Function [3]



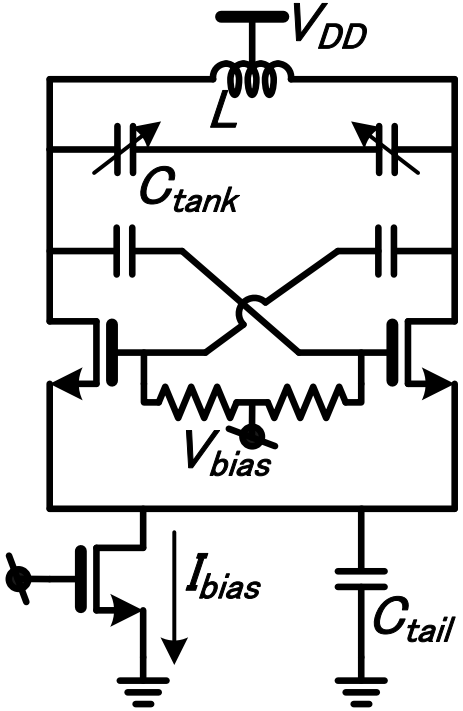
[3] A.Hajimiri and T.H.Lee, JSSC 1998

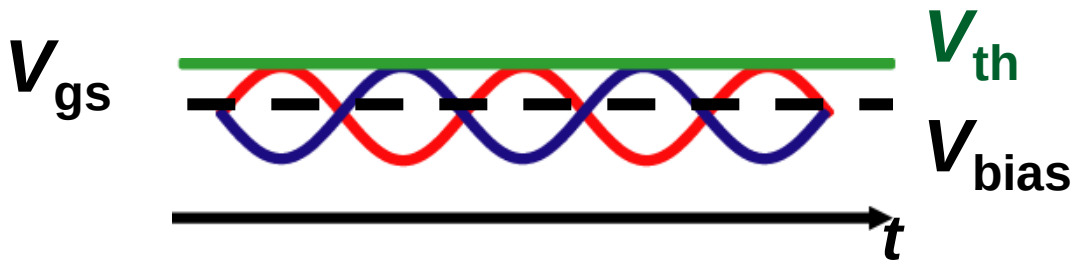
Operation of Class-C VCO





Startup problem





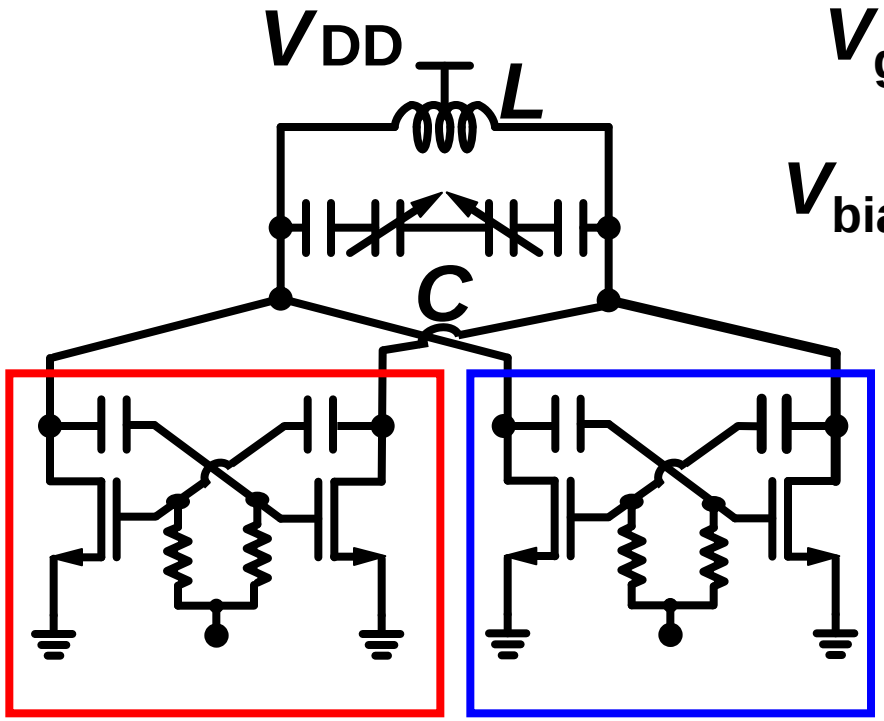
$$V_{\text{bias}} + A_{\text{t}} > V_{\text{th}}$$

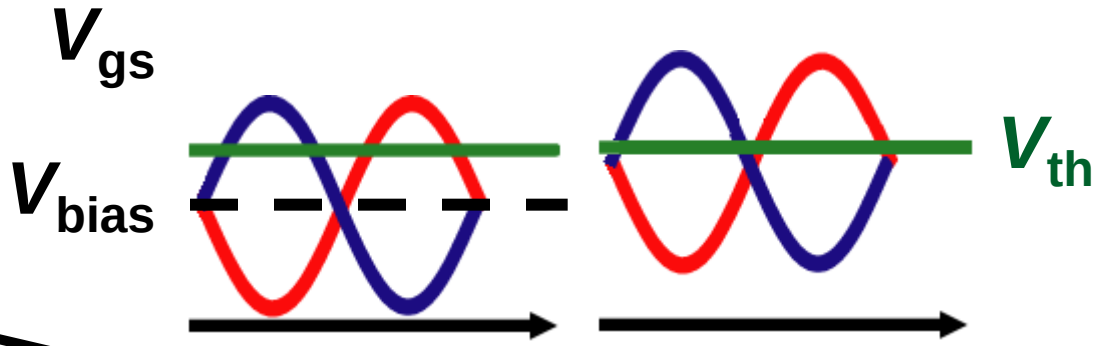
$$A_{\text{t}} > V_{\text{th}} - V_{\text{bias}}$$

At low supply voltage,
the amplitude is **very small.**

The oscillation is not robust.

Dual-Conduction Class-C VCO[4]



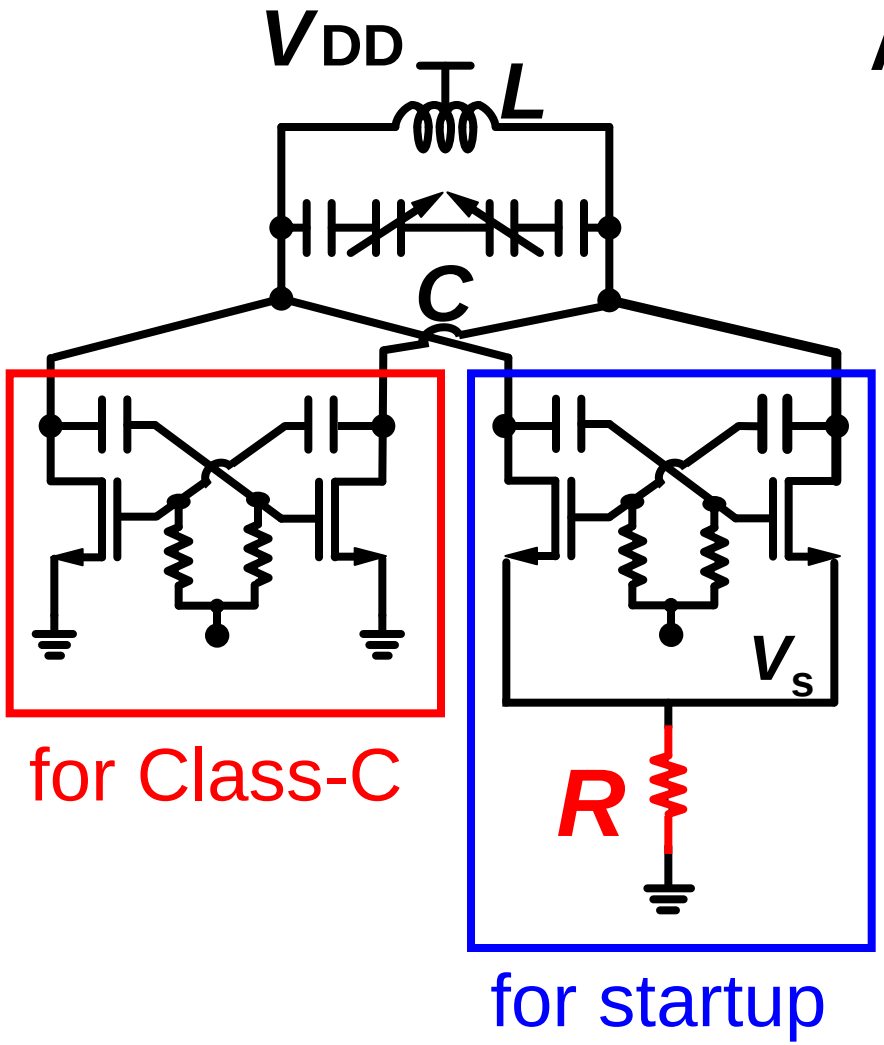


☺ It works at 0.2 V supply voltage.

☹ The pair for startup consumes power and degrades phase noise.

[4] K.Okada, *et al., VLSIC 2009*

Solution



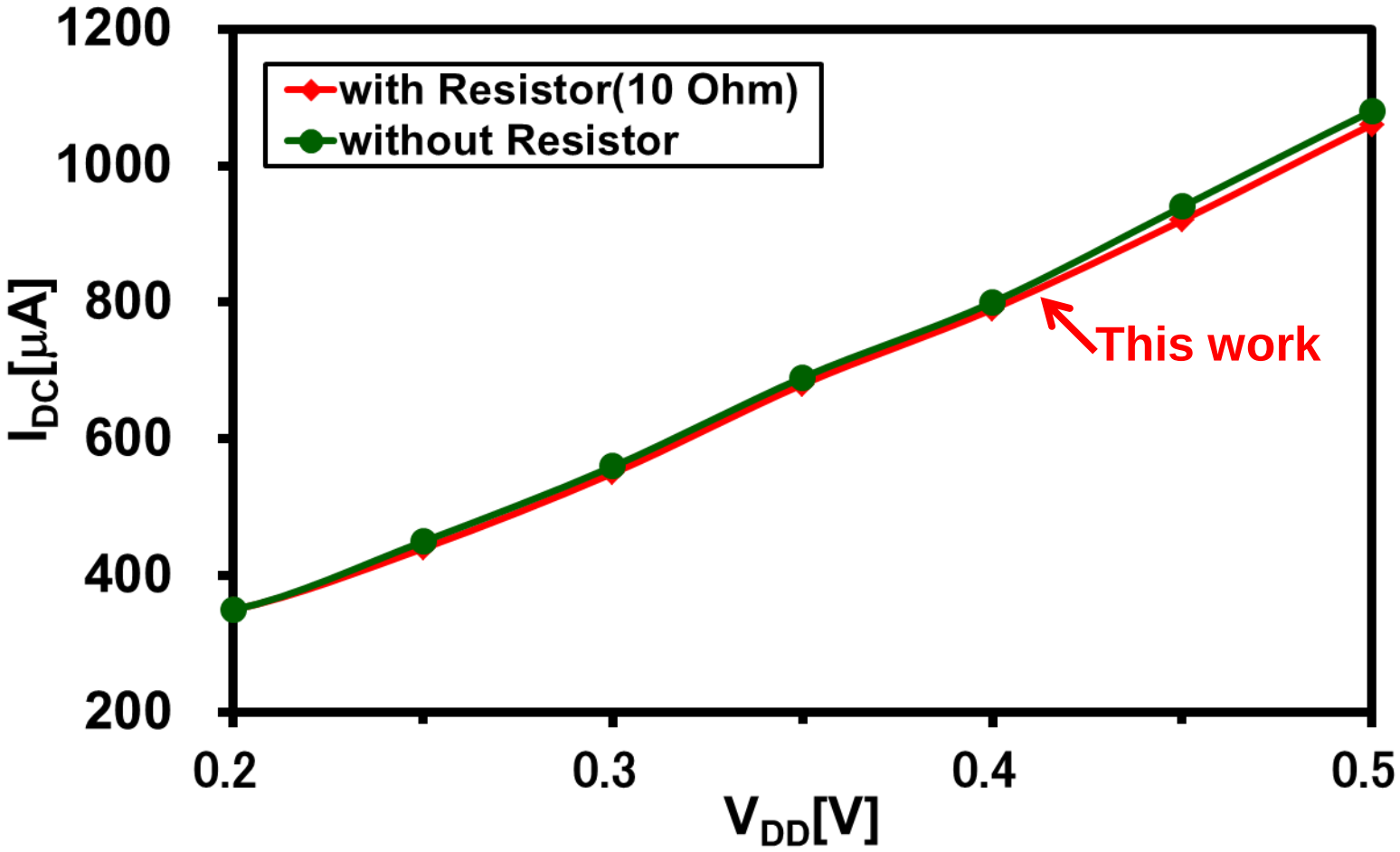
Add a resistor to the Source

V_s rise ⇒ V_{gs}, V_{ds} fall

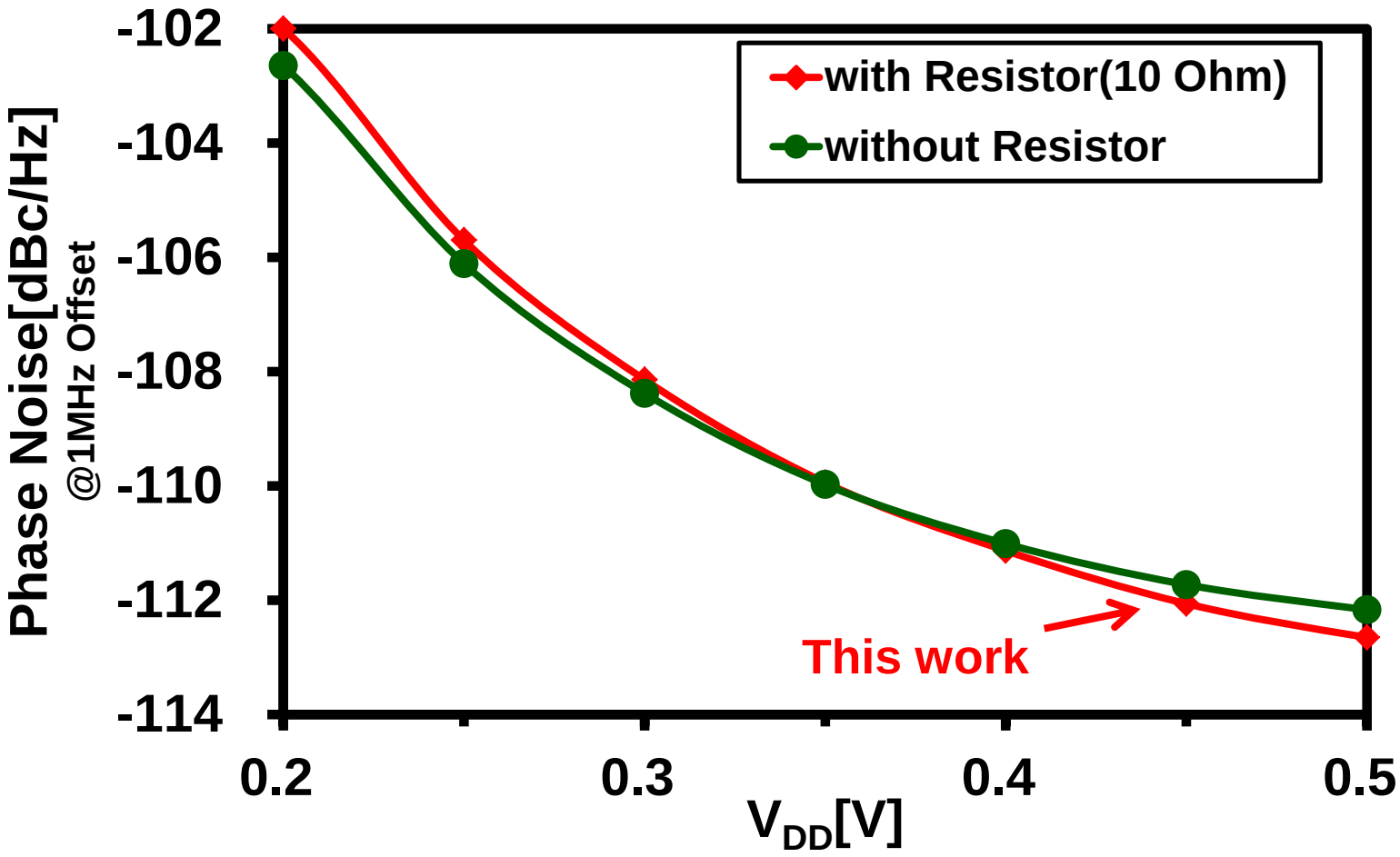
$$I_{ds} \approx \frac{\mu C_{ox}}{2}\left(V_{gs} - V_{th}\right)^2\left(1 + \frac{V_{ds}}{V_A}\right)$$

I_{ds} for startup pair decrease

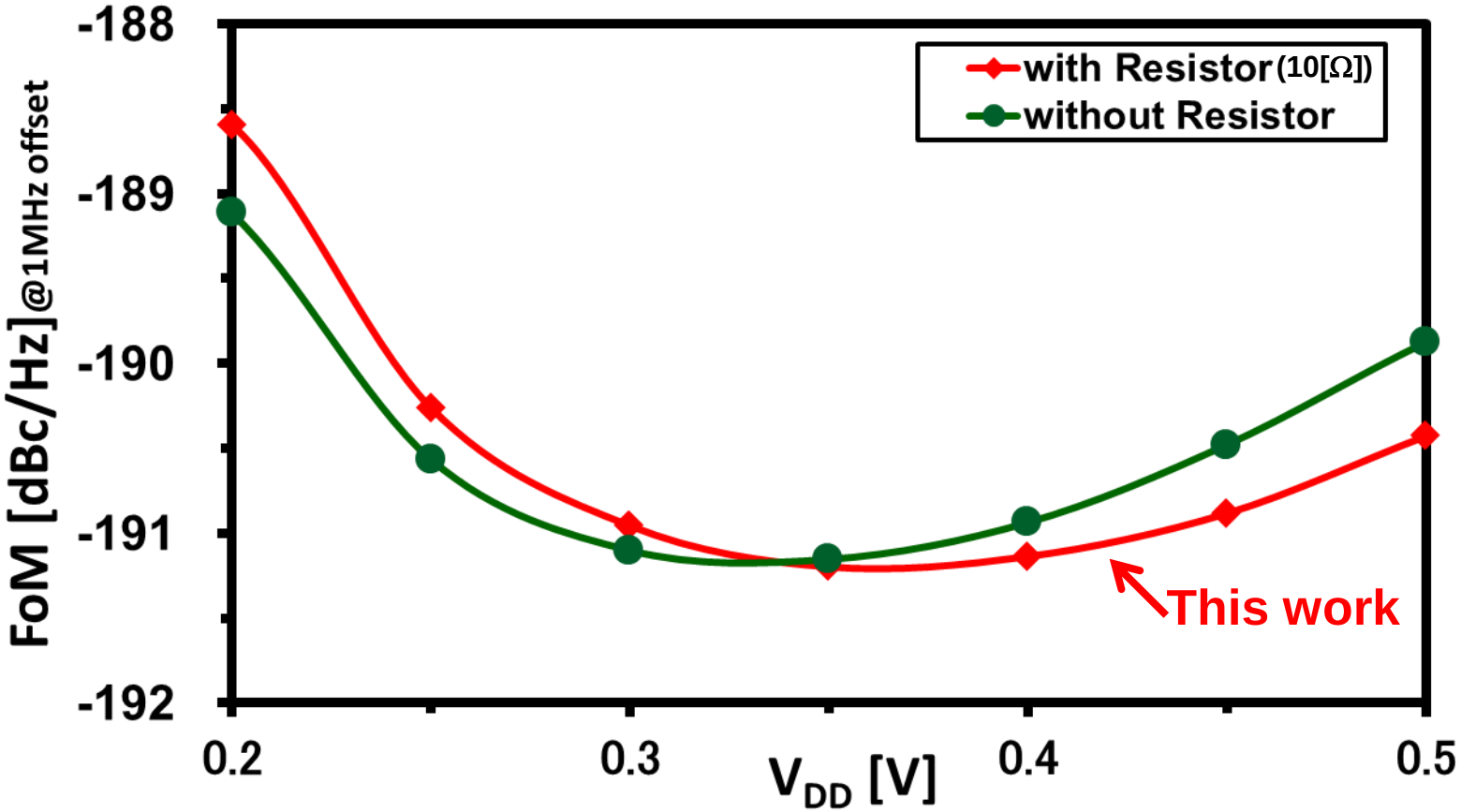
Simulation result



Simulation result

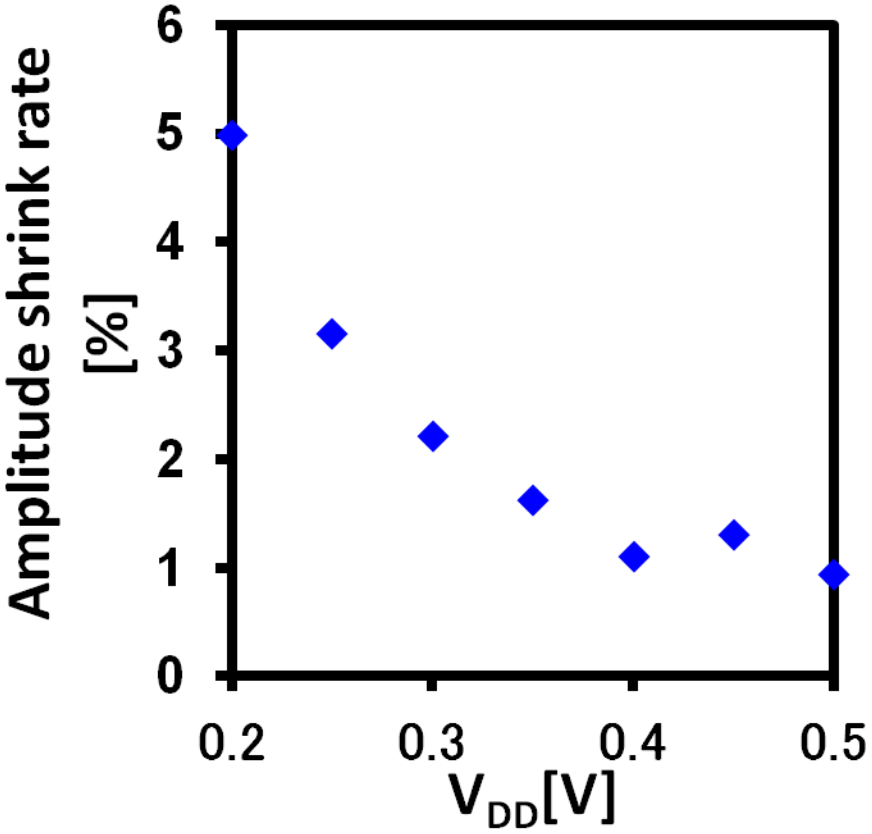


Simulation result



$$\mathrm{FoM} = \mathcal{L}(f_{\mathrm{offset}}) - 20\log\left(\frac{f_0}{f_{\mathrm{offset}}}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\ [\mathrm{mW}]}\right)$$

Simulation result

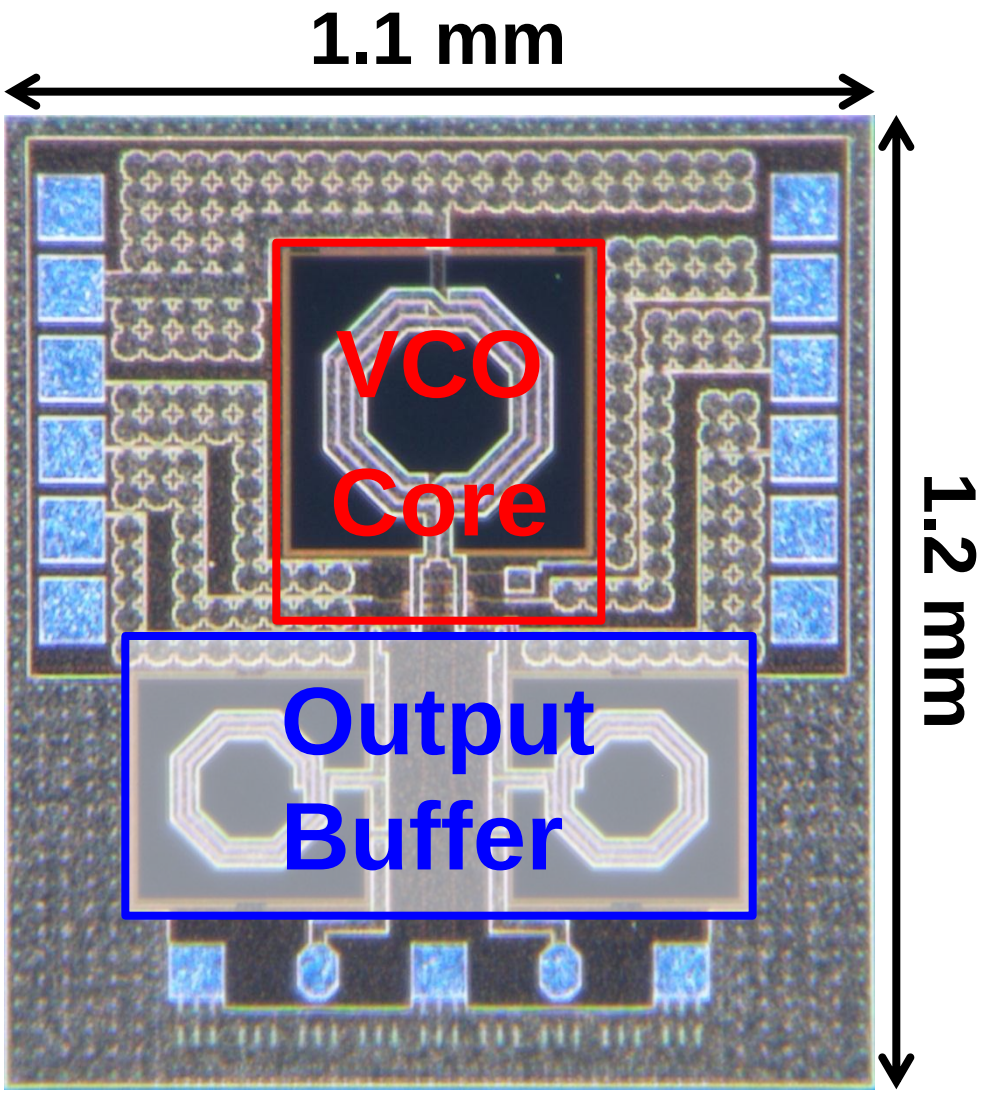


$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2kT}{P_{sig}}\cdot\left(\frac{f_0}{2Q\Delta f}\right)^2\right]$$

Amplitude shrink degrades phase noise and FoM

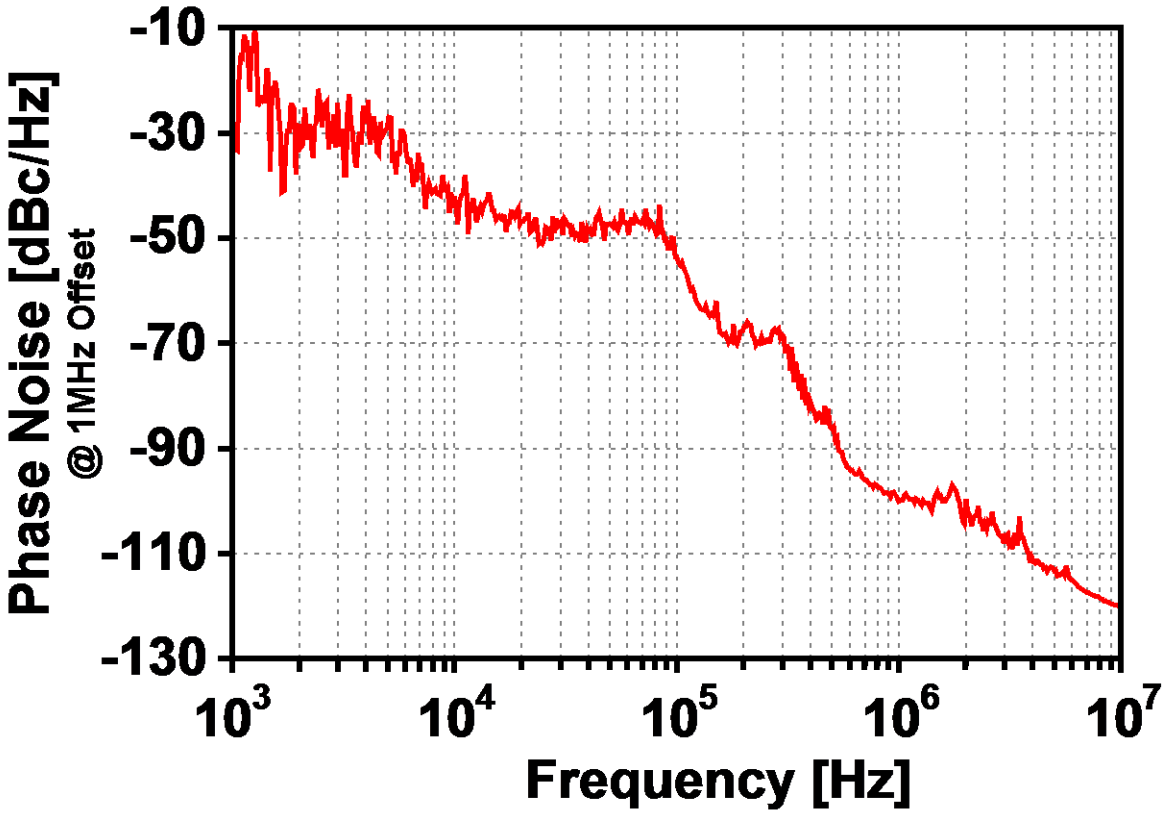
$$\text{Amplitude shrink rate}[\%] = \frac{At(0\Omega) - At(10\Omega)}{At(0\Omega)} \times 100$$

Chip micrograph



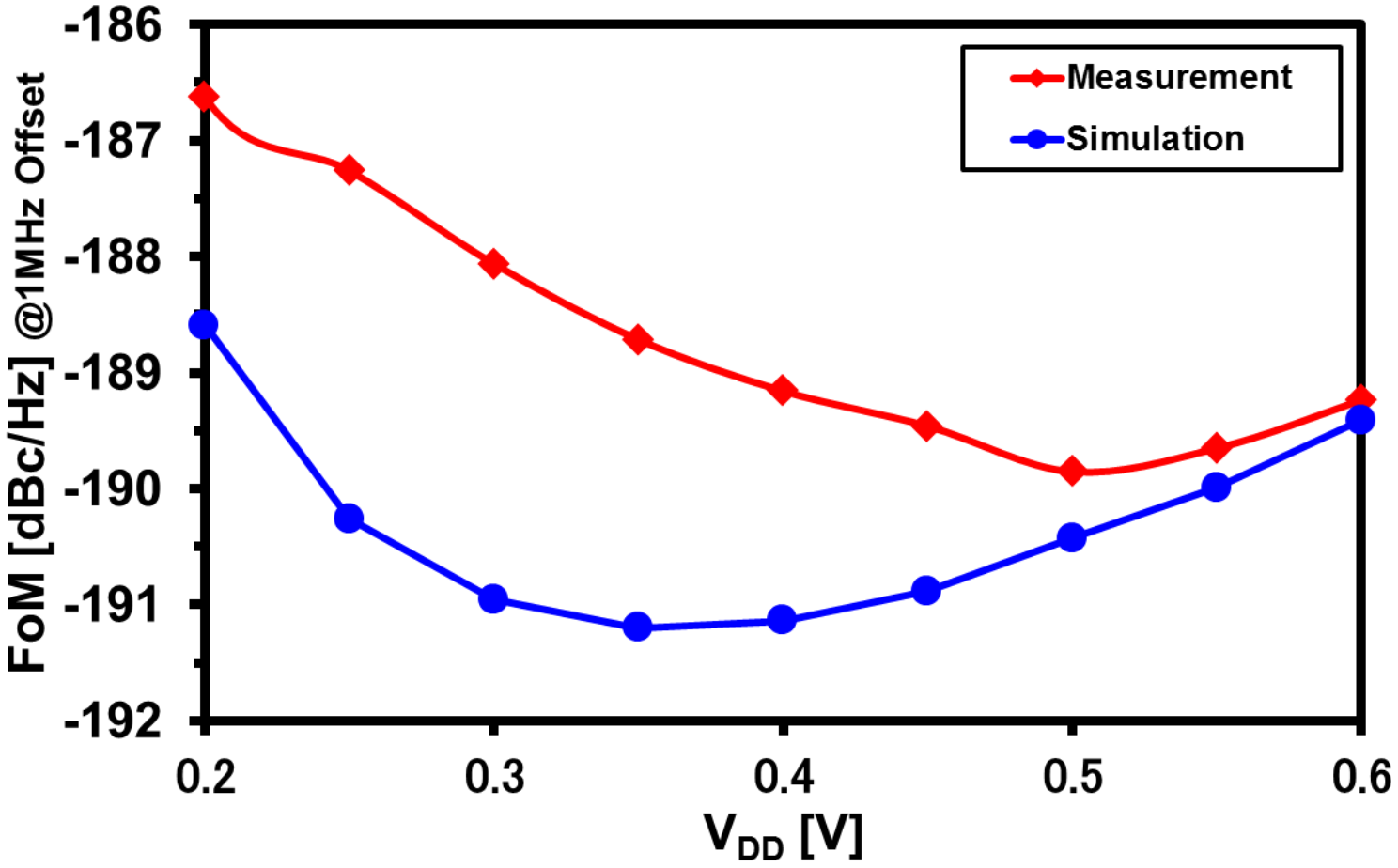
- CMOS 180 nm
- Core size 0.20 mm^2
- 10 Ohm tail resistor

Measurement result



V_{DD}	0.2 V
Frequency	5.4 GHz
Phase Noise	-102 dBc/Hz @1MHz Offset
Power	**96 μW**
FoM	-187 dBc/Hz

Measurement result



Performance summary

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	[3]	[5]		[4]		This work	
Technology	CMOS 0.13μm	CMOS 0.18μm		CMOS 0.18μm		CMOS 0.18μm	
Supply voltage [V]	1.0	0.50	0.35	0.30	0.20	0.50	0.20
DC Power [μW]	1300	570	1460	159	114	630	**96**
Frequency [GHz]	4.9	3.8	1.4	4.5		5.4	
Phase noise [dBc/Hz]	-130 @3MHz offset	-119 @1MHz offset	-129 @1MHz offset	-109 @1MHz offset	-104 @1MHz offset	-113 @1MHz offset	-102 @1MHz offset
FoM [dBc/Hz]	-196	-193	-190	-190	-187	-190	-187
Topology	Class-C (single)	Transformer feedback		Dual-Conduction Class-C		Dual-Conduction Class-C	

[3] A. Mazzanti, *et al*., JSSC 2008
[4] K.Okada, *et al., VLSIC 2009*
[5] K.Kwok, *et al., JSSC 2005*

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Conclusion

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- **We added a resistor to the source of transistors for startup of Dual-Conduction Class-C VCO.**
- **In the simulation, it reduced power consumption and improved phase noise in more than 0.35 V supply voltage.**
- **We fabricated the proposed VCO. It operates at 0.2V supply voltage and consumes only 96 μW.**

End

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Thank you for your attention

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