A 60 GHz CMOS Power Amplifier Using Capacitive Cross-Coupling Neutralization with 16% PAE

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Outline

- **Back Ground**
- **Capacitive Cross-Coupling Neutralization**
- **3-stage Power Amplifier**
- **Measurement Result**
- **Conclusion**

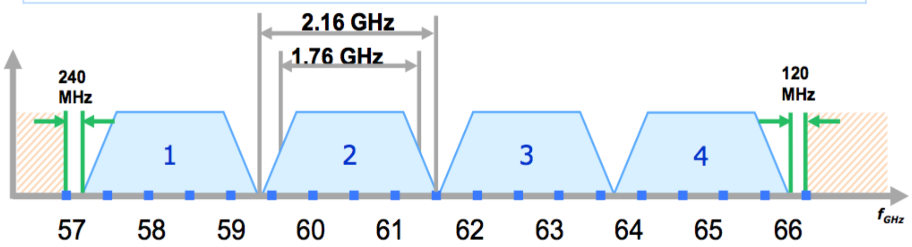
Motivation

60GHz CMOS direct-conversion transceiver for multi-Gbps wireless communication

IEEE 802.15.3c specification

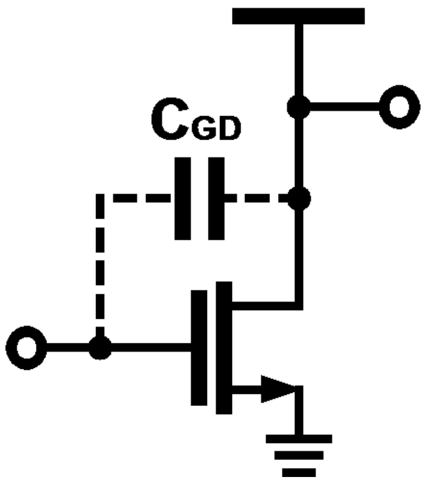
- 57.24GHz - 65.88GHz
- 2.16GHz/ch x 4channels
- QPSK → 3.5Gbps/ch
- 16QAM → 7.0Gbps/ch

Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (GHz)	Roll-Off Factor
A1	57.24	58.32	59.40	1.76	0.227
A2	59.40	60.48	61.56	1.76	0.227
A3	61.56	62.64	63.72	1.76	0.227
A4	63.72	64.80	65.88	1.76	0.227

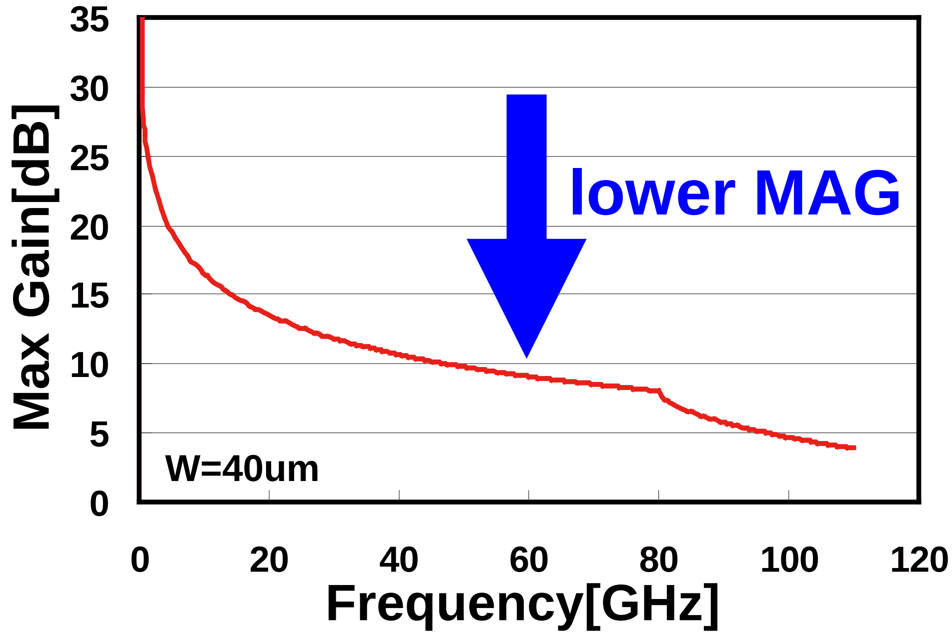


Challenges for 60GHz PA

Parasitic Capacitance

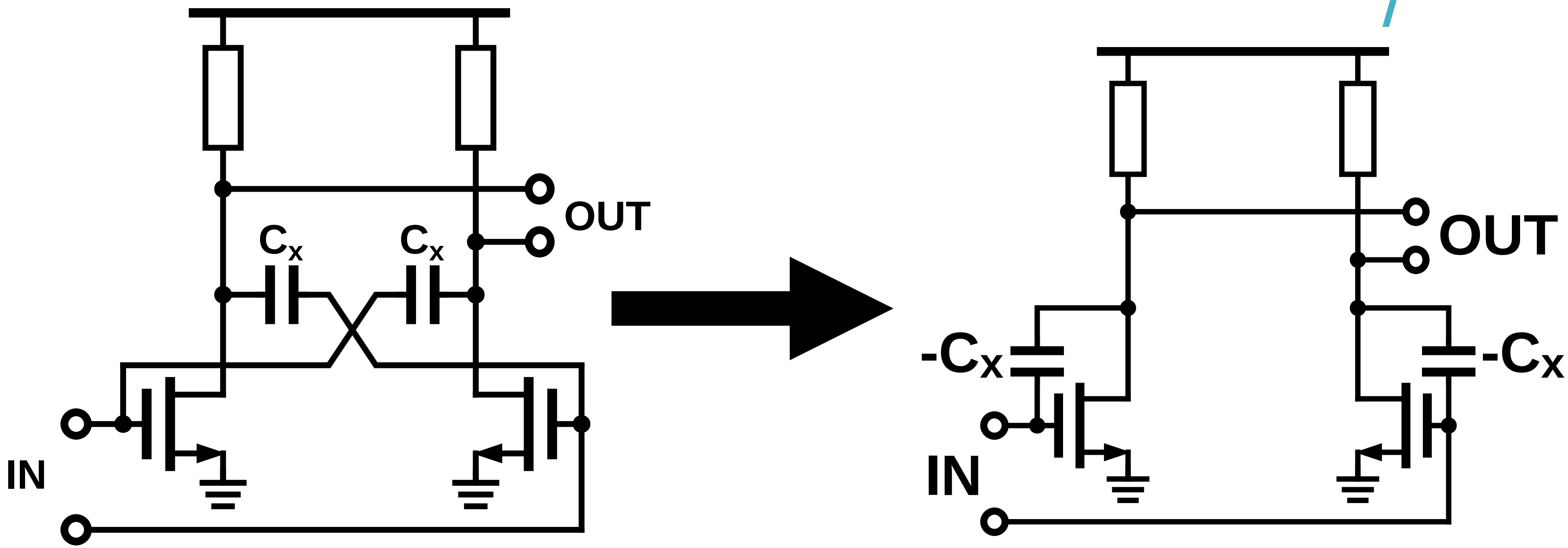


$$C_{GD} = -\frac{\mathrm{Im}[Y_{12}]}{j\omega}$$



- **Parasitic Capacitances causes low reverse isolation.**

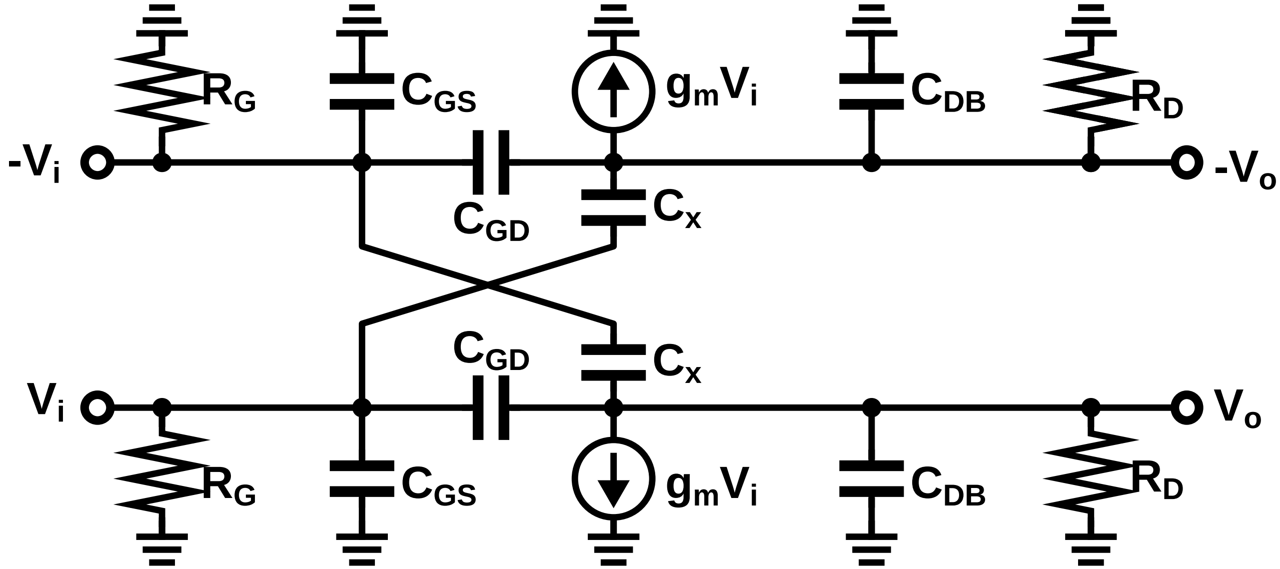
Capacitive Cross Coupling[3]



- **A cross-coupled capacitor between gate and drain of the opposite-side transistor works as negative capacitor.**
  - **The reverse isolation is improved.**

[3] W.L. Chan, *et al*., ISSCC 2010

Small signal equivalent circuit



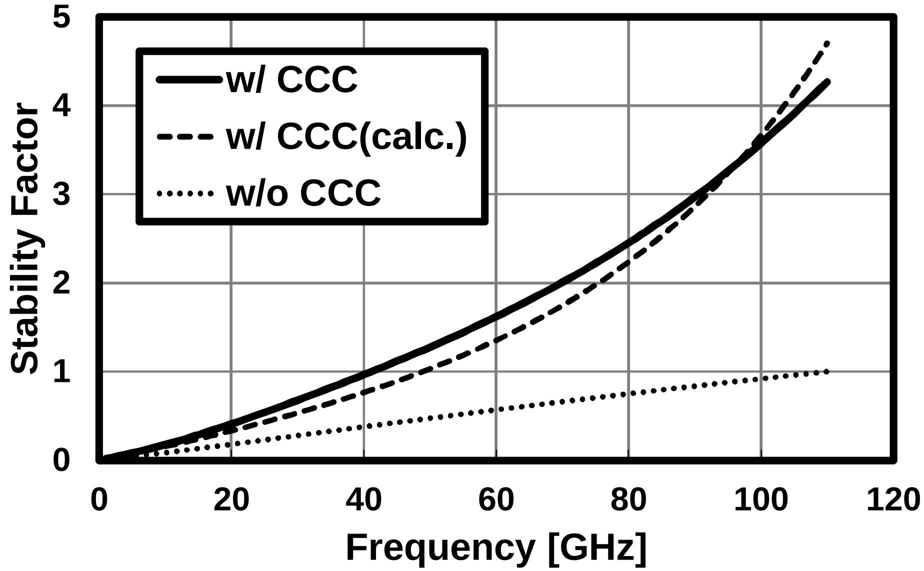
Stability

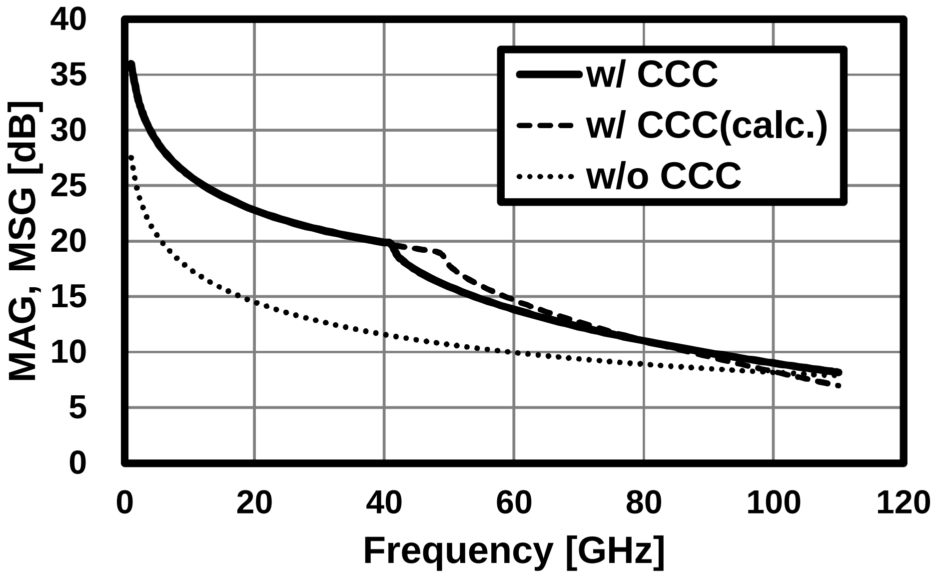
$$k = \frac{2\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}] - \mathrm{Re}[Y_{12}Y_{21}]}{|Y_{12}Y_{21}|} = \frac{2 + \omega^2 (C_{GD} - C_X)^2 R_G R_D}{\omega |C_{GD} - C_X| R_G R_D \sqrt{\omega^2 (C_{GD} - C_X)^2 + {g_m}^2}}$$

Maximum Available Gain

$$\mathrm{MAG} = \left|\frac{Y_{21}}{Y_{12}}\right| \left(k - \sqrt{k^2 - 1}\right) = \frac{\sqrt{\omega^2 (C_{GD} - C_X)^2 + {g_m}^2}}{\omega |C_{GD} - C_X|} \left(k - \sqrt{k^2 - 1}\right)$$

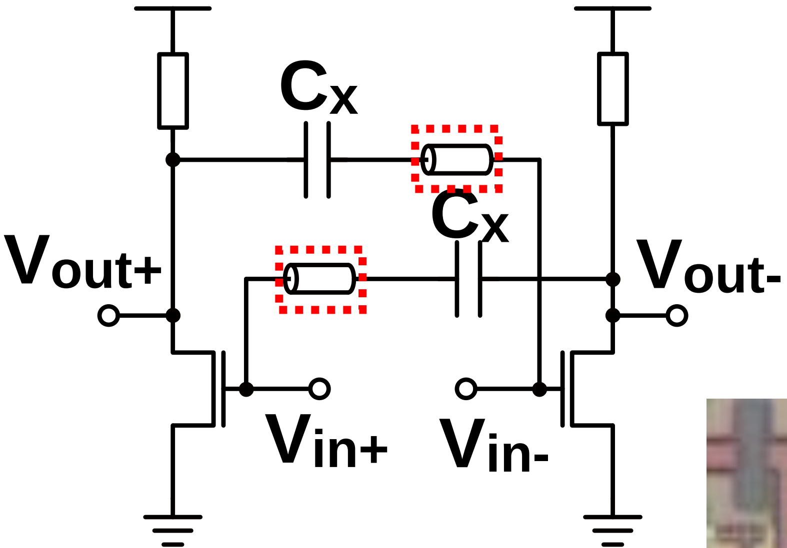
Simulation result

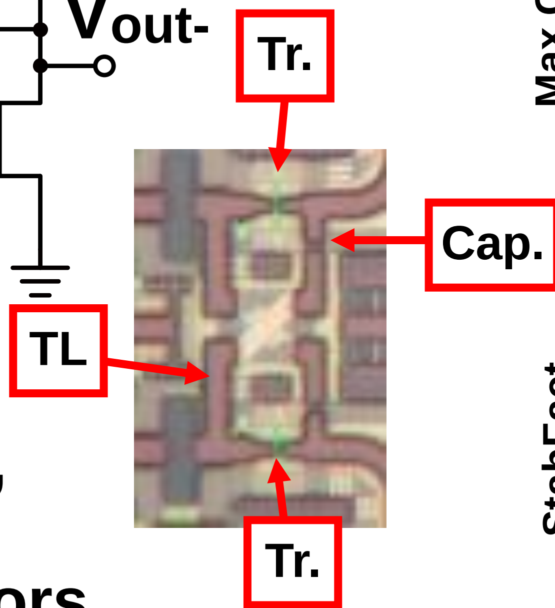




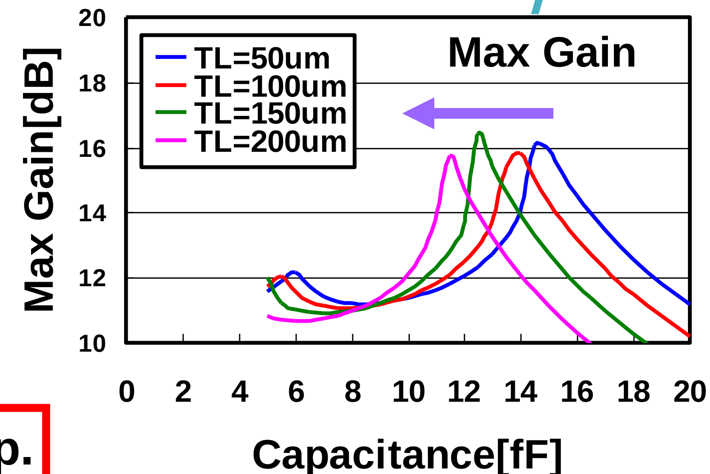
- **Stability Factor is improved across entire frequency.**
- **The maximum available gain is improved about 5dB at 60GHz**

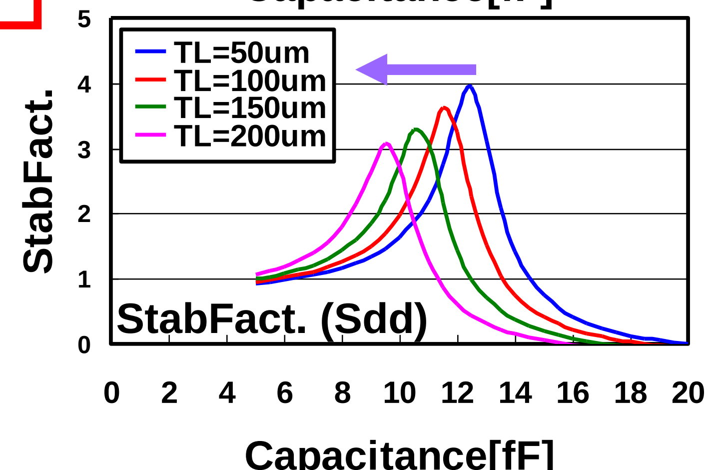
Influence of TL





In actual layout, TL is needed to connect 2 transistors.

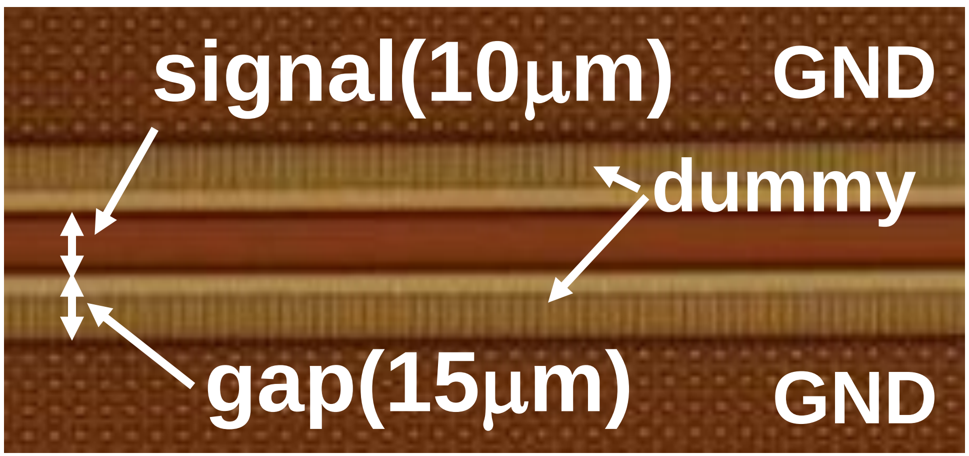


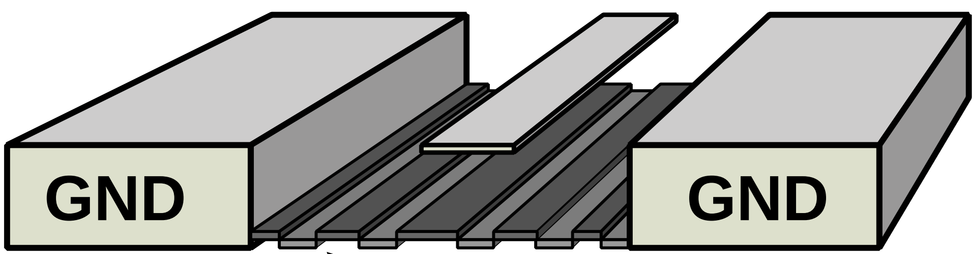


- **The longer TL, The smaller capacitance to cross-couple is needed.**

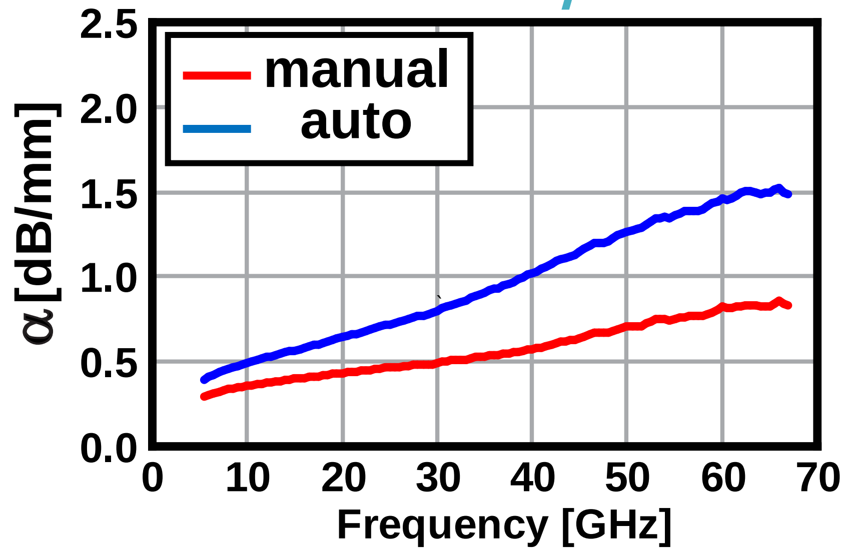
Transmission line

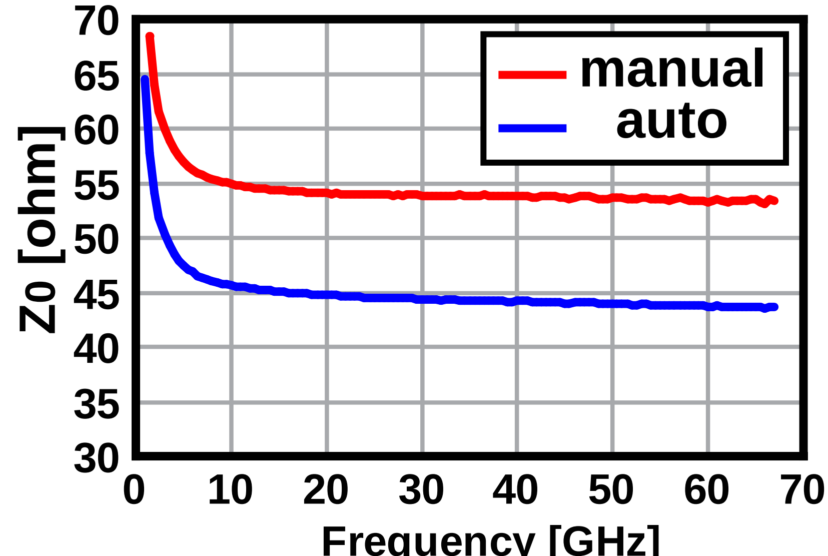
- **Low loss(0.8dB/mm)**
- **Dummy metals are manually placed.**





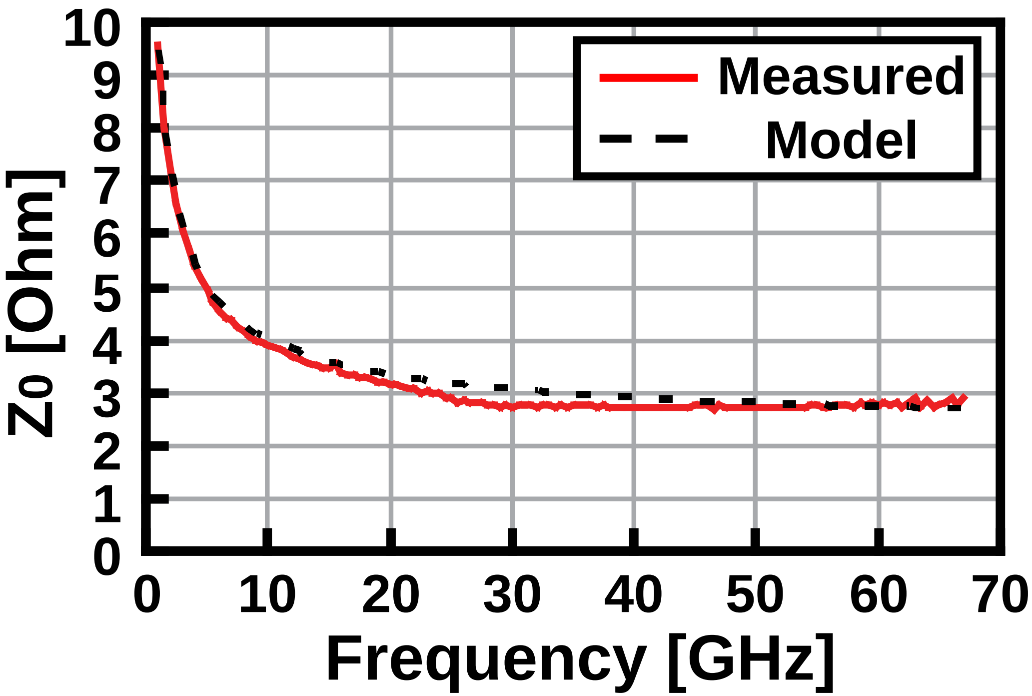
M1&M2 shield

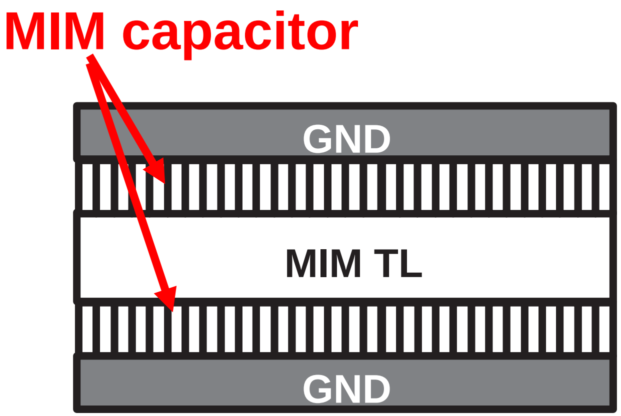




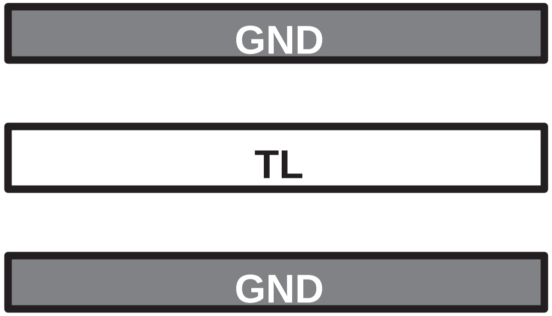
MIM Transmission Line

- De-coupling use
- Modeling accuracy
- Avoiding self-resonance of parallel-plate capacitors





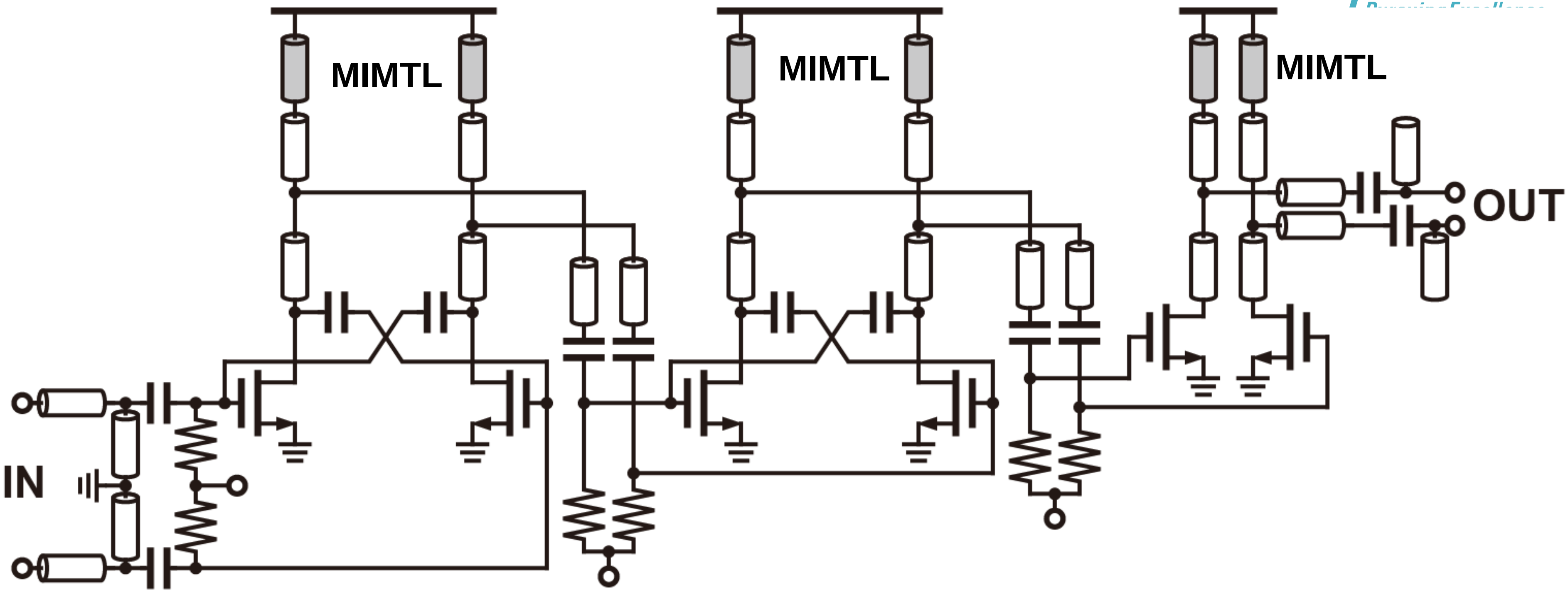
MIM transmission line



50Ω transmission line

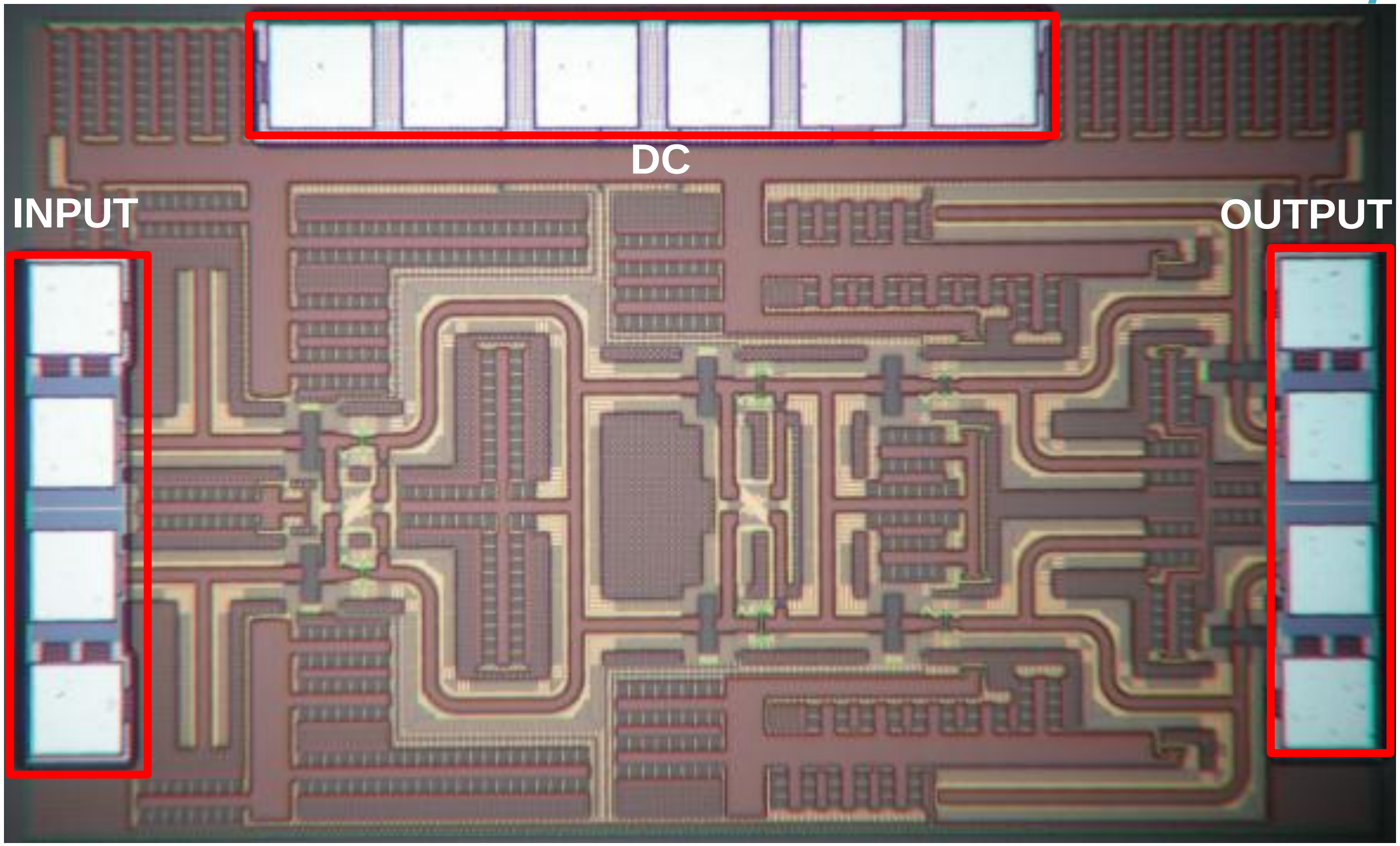
 [4] T. Suzuki, *et al.*, ISSCC 2008

Schematic of PA



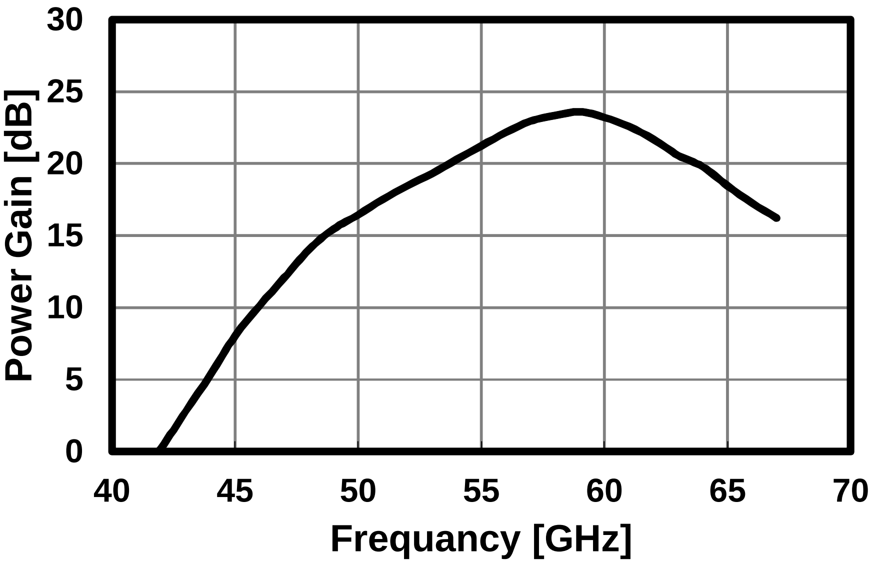
- 3-stage differential power amplifier.
- The capacitive cross-coupling neutralization is used.
- The guided micro-strip line is used for matching network.
- The de-coupling is implemented as MIM TL.

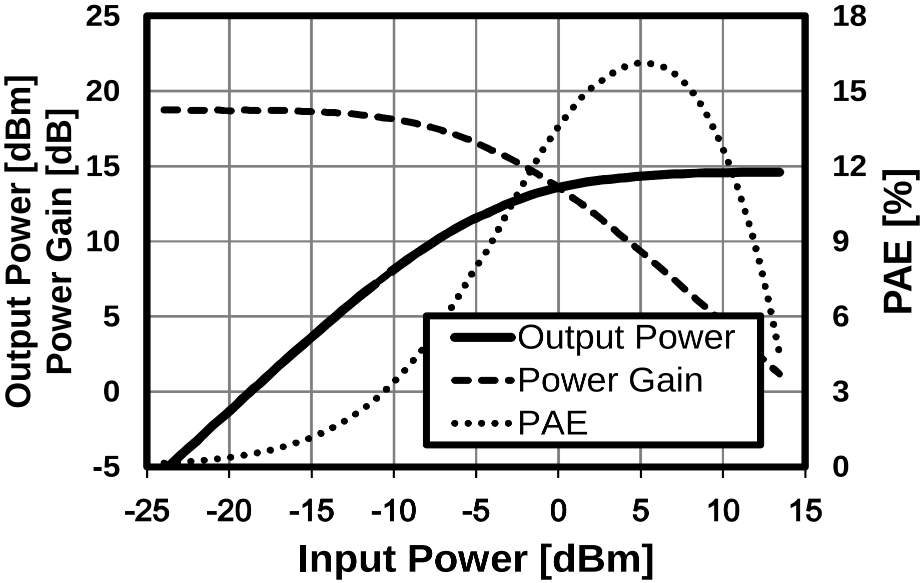
Die photo



- **Core area: 1.0mmx0.6mm**

Measurement result





- **Power Gain: 23.2dB**
- **P_{sat}: 14.6dBm**
- **P_{1dB}: 10.0dBm**
- **Power Consumption: 135mW (V_{dd}=1.2V)**
- **Peak PAE: 16.3%**

Performance comparison

	Power Gain [dB]	P_{1dB} [dBm]	P_{sat} [dBm]	Peak PAE [%]	Power [mW]	V_{DD} [V]
ISSCC 2008[5]	5.5	9	12.3	8.8	-	1.0
ISSCC 2009[3]	16	2.5	11.5	11	43.5	1.0
ISSCC 2010[6]	20.6	18.2	19.9	14.2	-	1.2
ISSCC 2010[7]	19.2	14.1	17.7	11.1	480	1.0
ISSCC 2010[8]	14.3	11	16.6	4.9	732	1.2
ISSCC 2011[9]	20.3	15	18.6	15.1	-	1.0
This Work	23.2	10.0	14.6	**16.3**	135	1.2

[5] D. Chowdhury, *ISSCC*, 2008 [6] C. Y. Law, *ISSCC*, 2010
[7] J. Lai, *ISSCC*, 2010 [8] B. Martineau, *ISSCC*, 2010 [9] J.Chen, *ISSCC*, 2011

Conclusion

- **A 60GHz power amplifier using the capacitive cross-coupling neutralization with the low-loss transmission line is presented.**

- **The 3-stage differential power amplifier in 65nm CMOS achieves power gain of 23.2dB, output power at 1-dB compression point of 10.0dBm, saturated output power of 14.6dBm, peak PAE of 16.3% and power consumption of 135mW.**