A 60GHz 16Gb/s 16QAM Low-Power Direct-Conversion Transceiver Using Capacitive Cross-Coupling Neutralization in 65nm CMOS

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Outline

- Motivation
- Previous Work
- Challenges for 60GHz Transceiver
- Capacitive Cross-Coupling Neutralization
- Transceiver Design
- Measurement Results
- Conclusion

Motivation

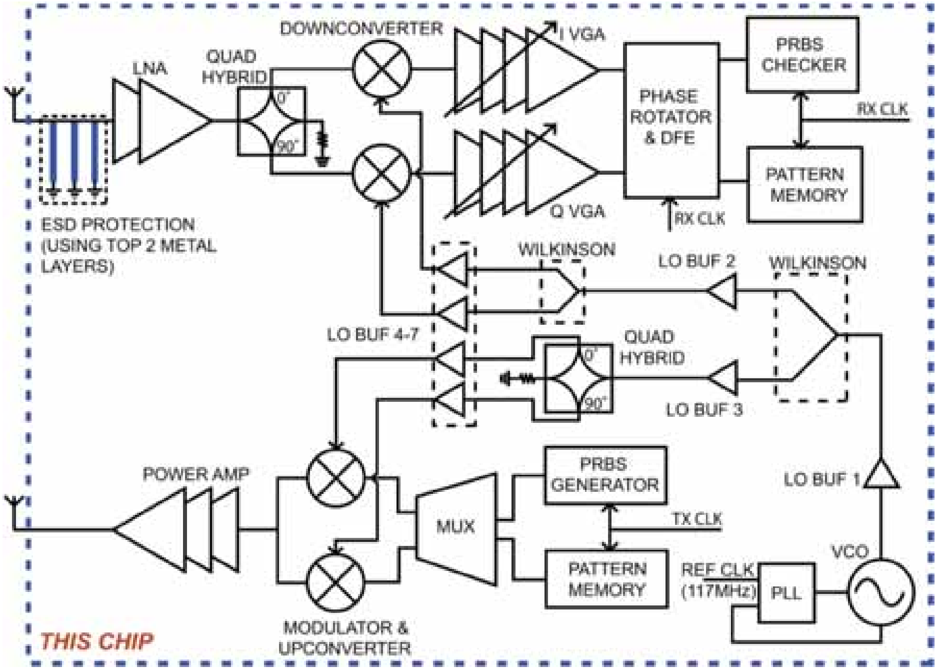
- **60GHz CMOS direct-conversion transceiver for multi-Gbps wireless communication**

IEEE 802.15.3c specification

- ■ **57.24GHz - 65.88GHz**
- ■ **2.16GHz/ch x 4channels**
- ■ **QPSK → 3.5Gbps/ch**
- ■ **16QAM → 7.0Gbps/ch**

Previous work 1

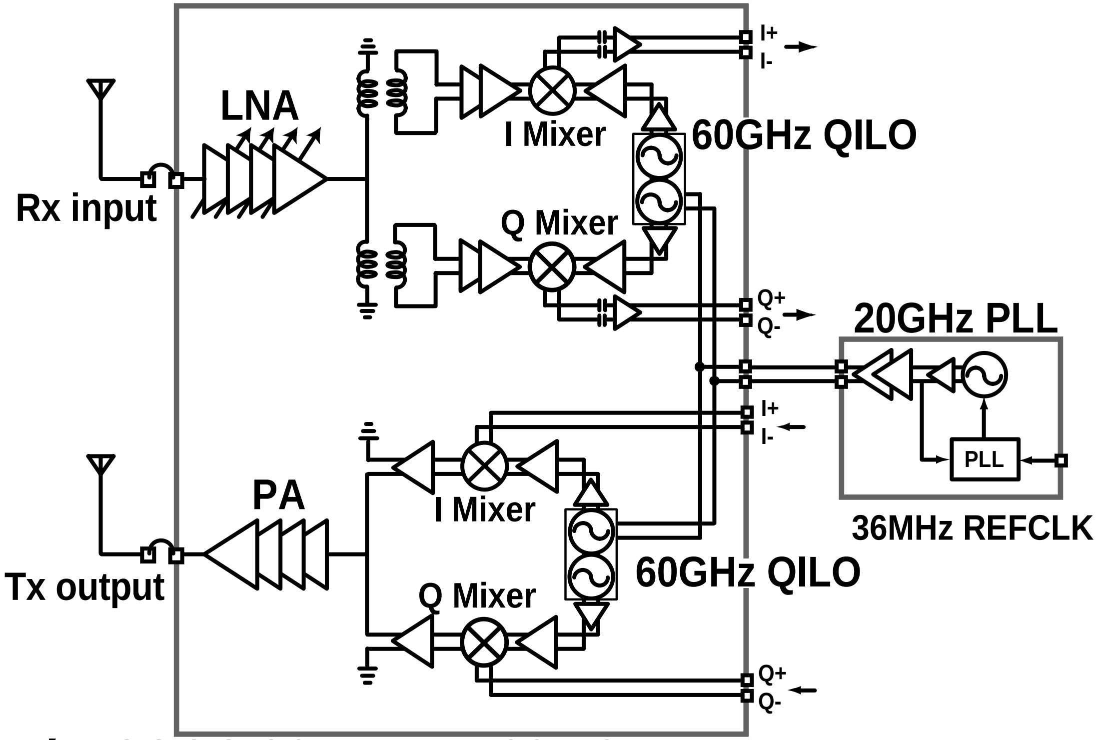
- **Direct-conversion transceiver by UCB[1]**
  - **90° hybrid is used to generate I/Q signal**
  - **4Gb/s for QPSK(Ch2)**
  - **16QAM is unsupported**



[1] C. Marcu, *et al*., *ISSCC* 2009, pp. 314-315

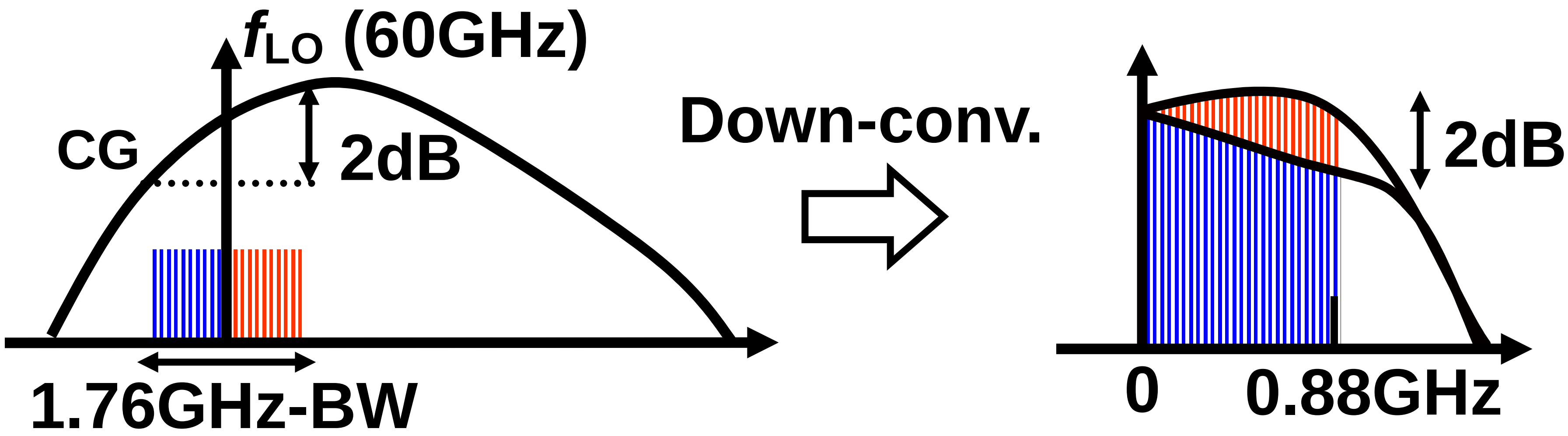
Previous work 2

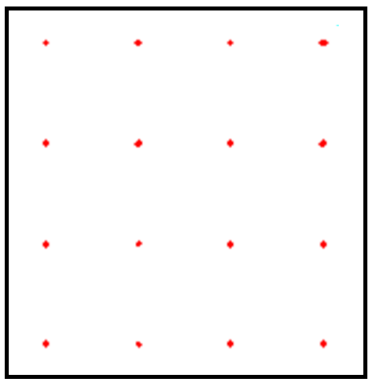
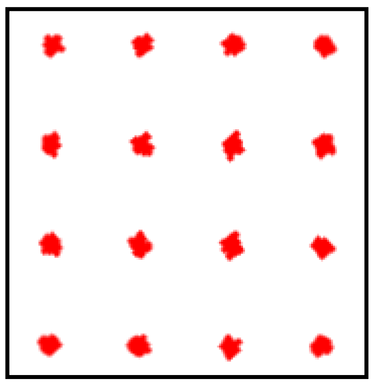
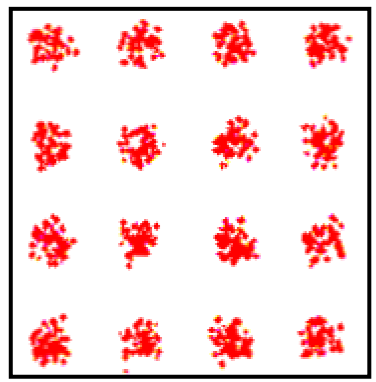
- **Direct-conversion transceiver by Tokyo Tech[2]**
  - **Quadrature LO is used to generate I/Q signal**
  - **11Gb/s for 16QAM(Ch2)**
  - **Not fully-balanced design → large I/Q mismatch**



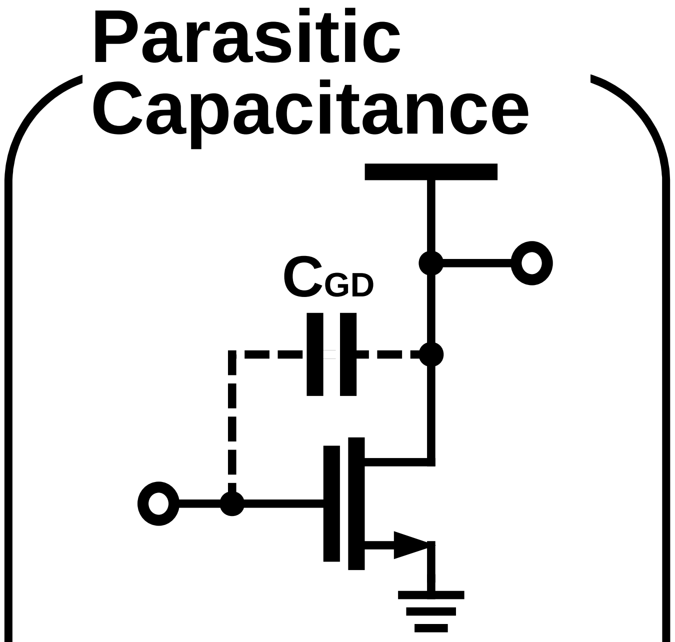
[2] K. Okada., *et al.*, *ISSCC 2011*, pp. 160-161

Gain Flatness at RF band

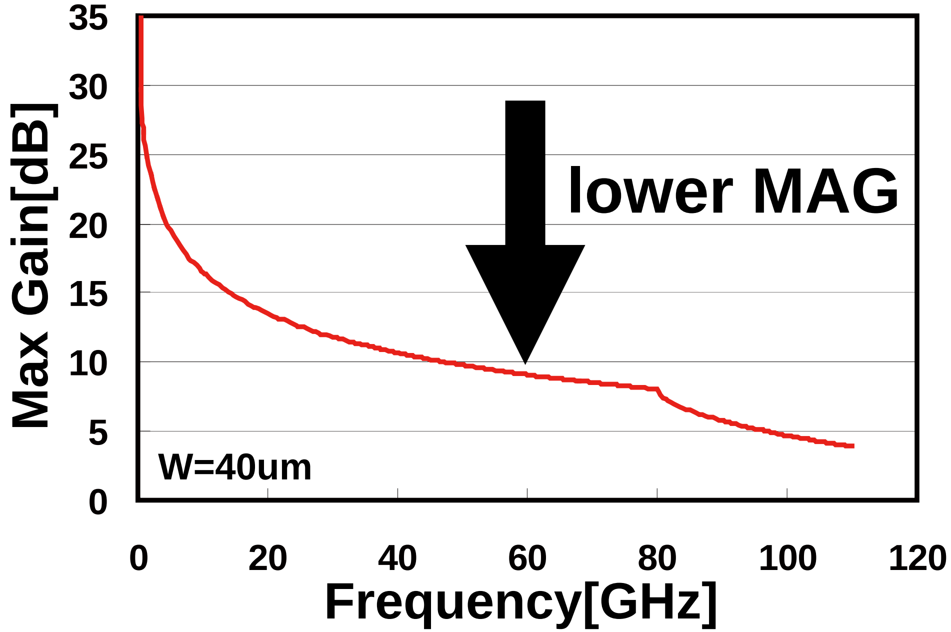


Gain Flatness	0dB	1dB	2dB
EVM	-	-22dB	-18dB
Constellation			

Parasitic Capacitance

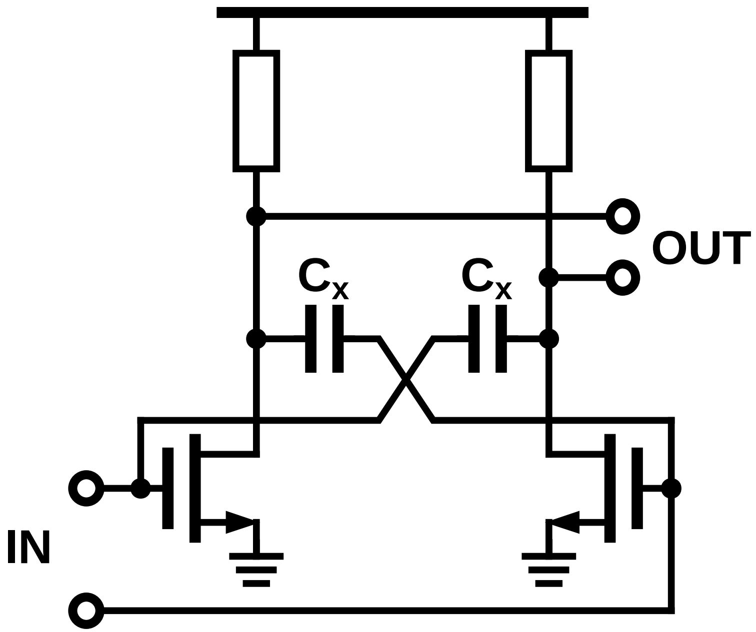


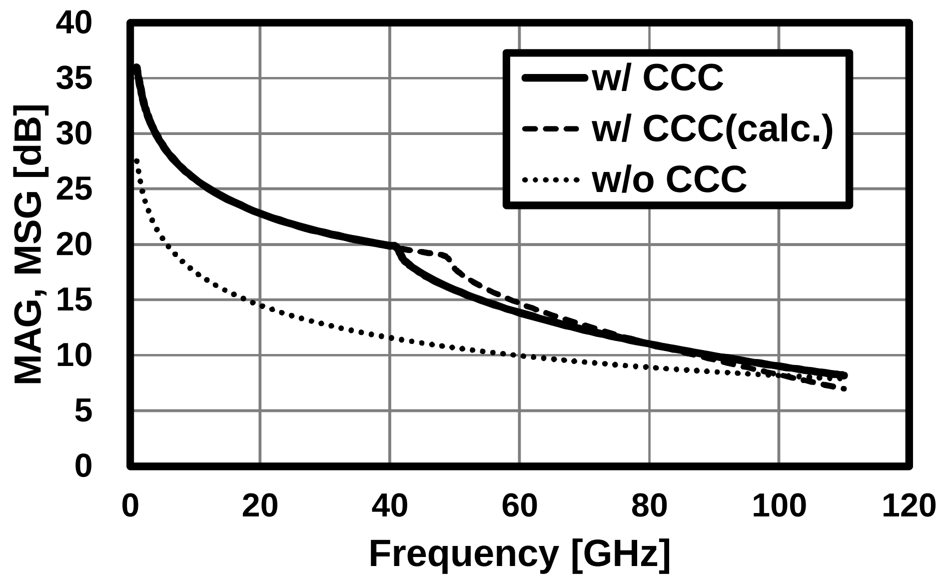
$$C_{GD} = -\frac{\mathrm{Im}[Y_{12}]}{j\omega}$$



- **Parasitic Capacitances causes low reverse isolation and low gain.**

Capacitive Cross-Coupling



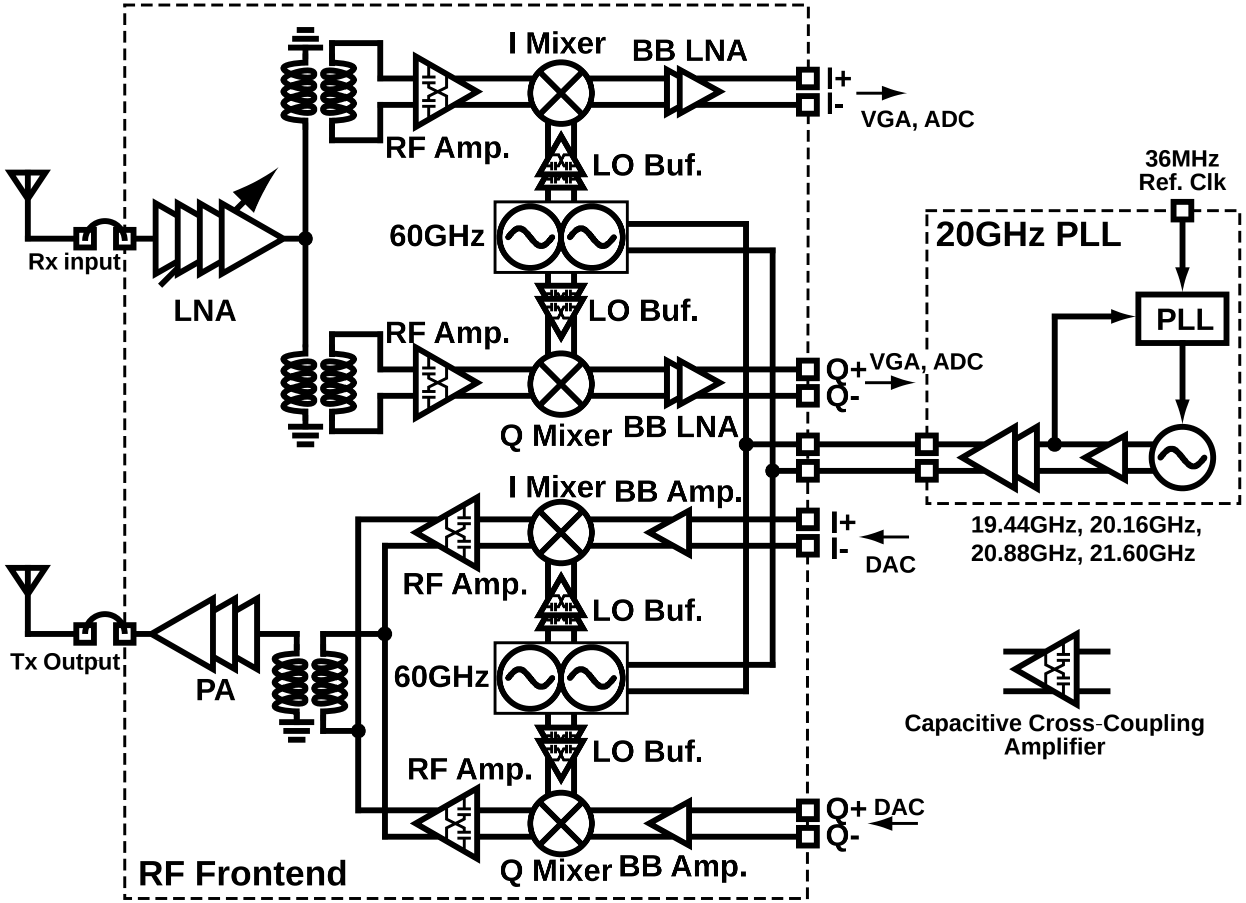


- **A cross-coupled capacitor between gate and drain of the opposite-side transistor works as negative capacitor.**
- **MAG is improved about 5dB at 60GHz**

[3] W.L. Chan, *et al*., ISSCC 2009

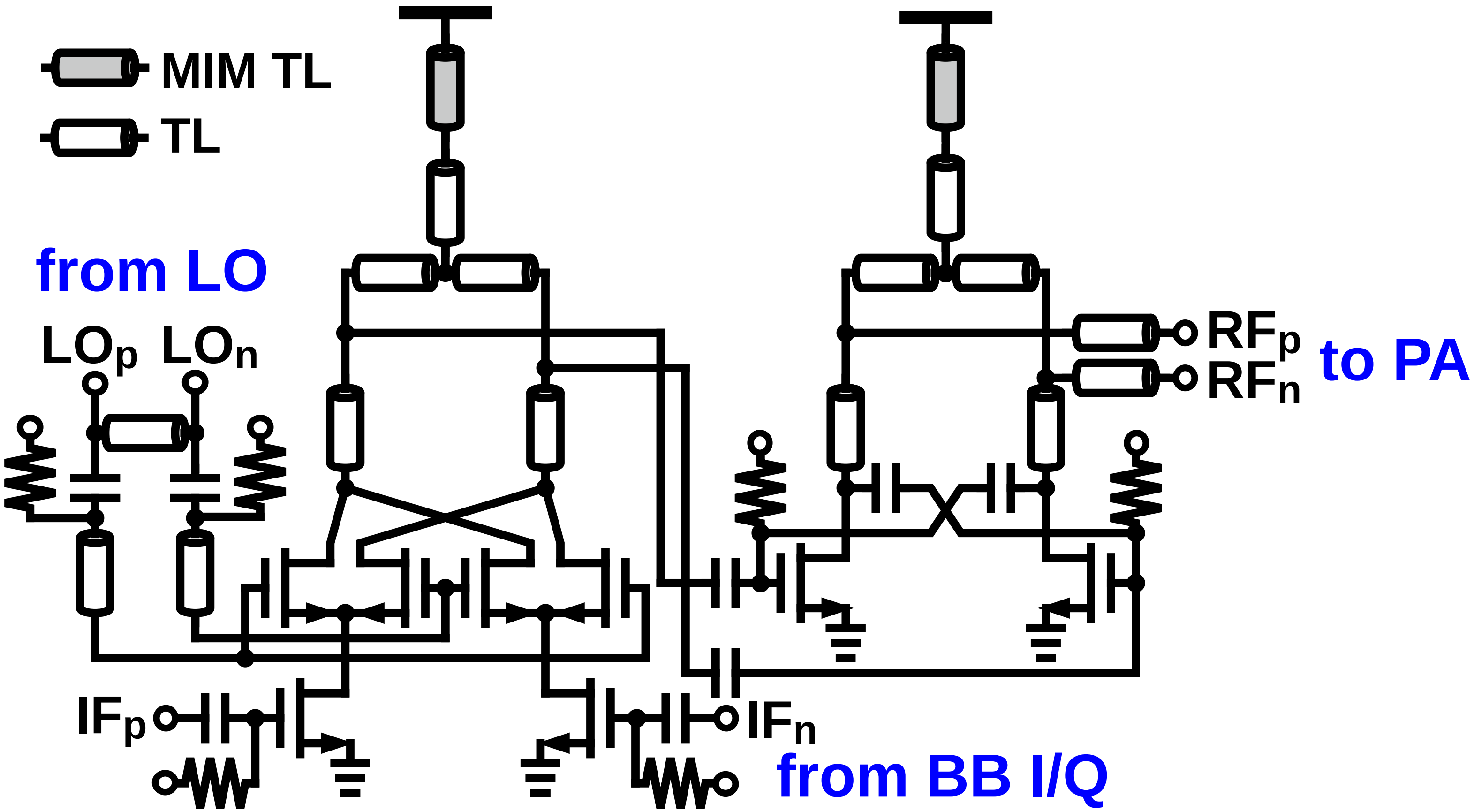
Direct-Conversion Architecture

- **Fully-balanced direct-conversion transceiver**
- **Capacitive cross-coupling neutralization**
- **Baseband LNA**



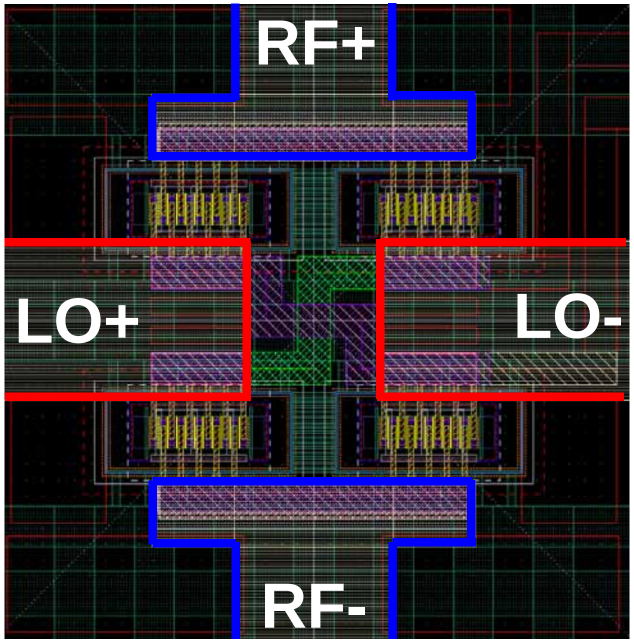
Up-Conversion Mixer

- Double-balanced Gilbert mixer
- Capacitive cross-coupling neutralization

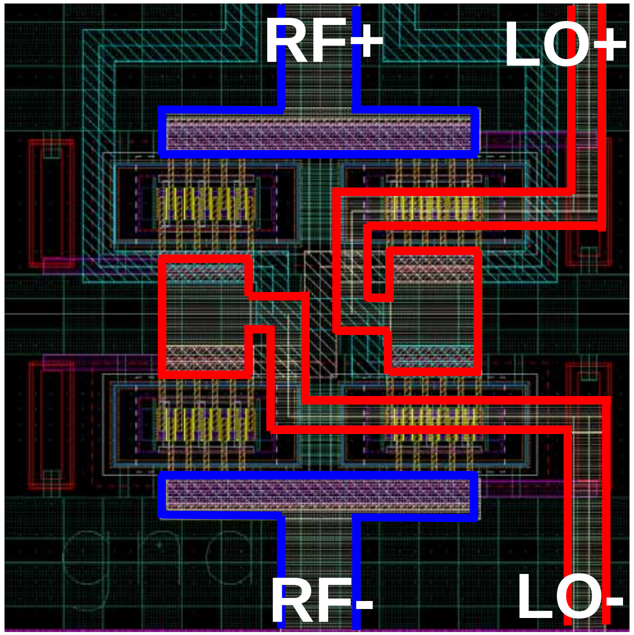


Mixer Core Layout

- **Mixer core excluding intersection**
  - LO line and RF line cross in matching network
- **Mixer core including intersection**
  - bad symmetrical property



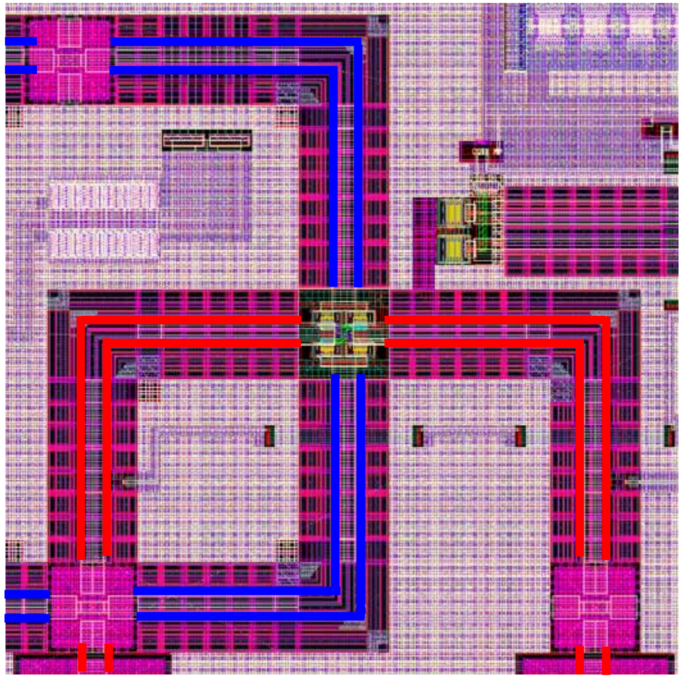
Symmetrical core (Not Good)



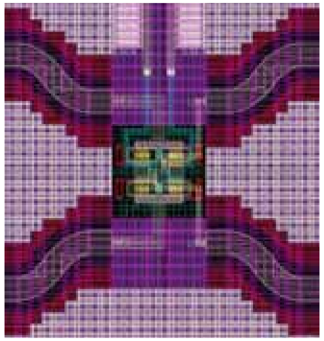
Asymmetrical core (Good)

Mixer Core Layout

- **Symmetrical core needs crossed and complicated matching network.**
- **Asymmetrical core can realize simple matching network.**



Symmetrical core



Asymmetrical core

SRR measurement

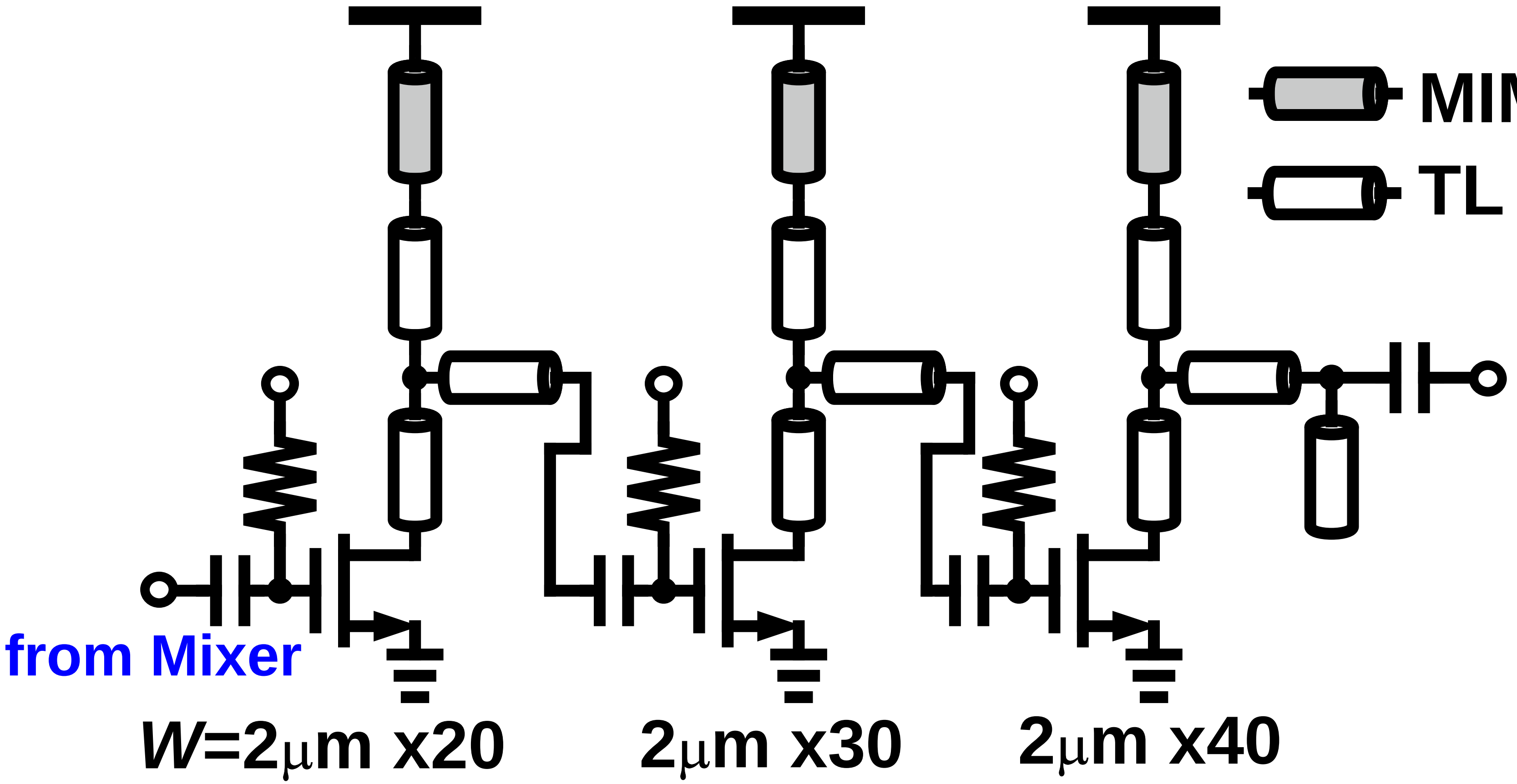
- **Asymmetrical core shows higher Sideband Rejection Ratio(SRR) and low I/Q mismatch**

	SRR	Amplitude Error	Phase Error
Symmetrical core	-24.5 [dB]	0.04[dB]	6.8[deg]
Asymmetrical core	-42.3[dB]	0.02[dB]	0.9[deg]

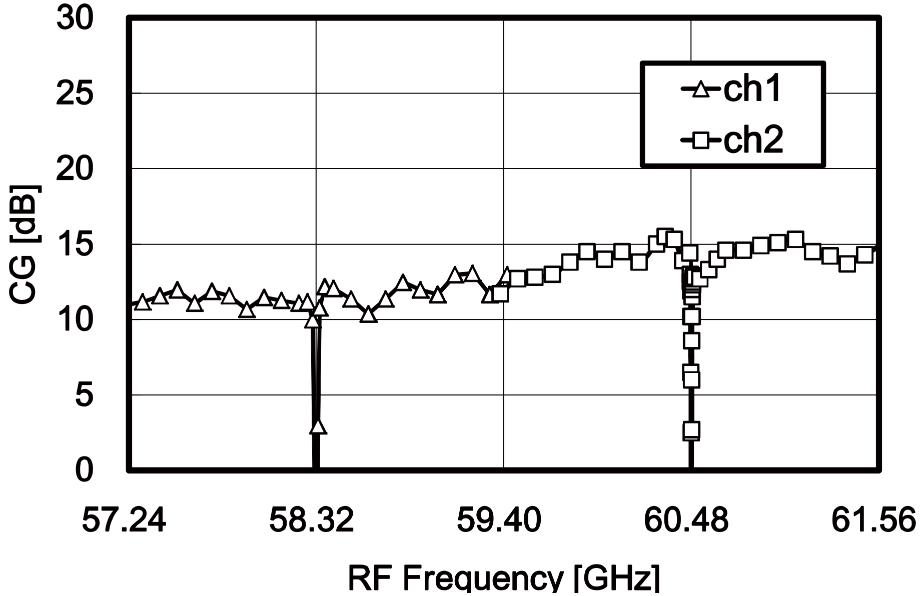
Simple layout of mixer can make I/Q mismatch negligible.

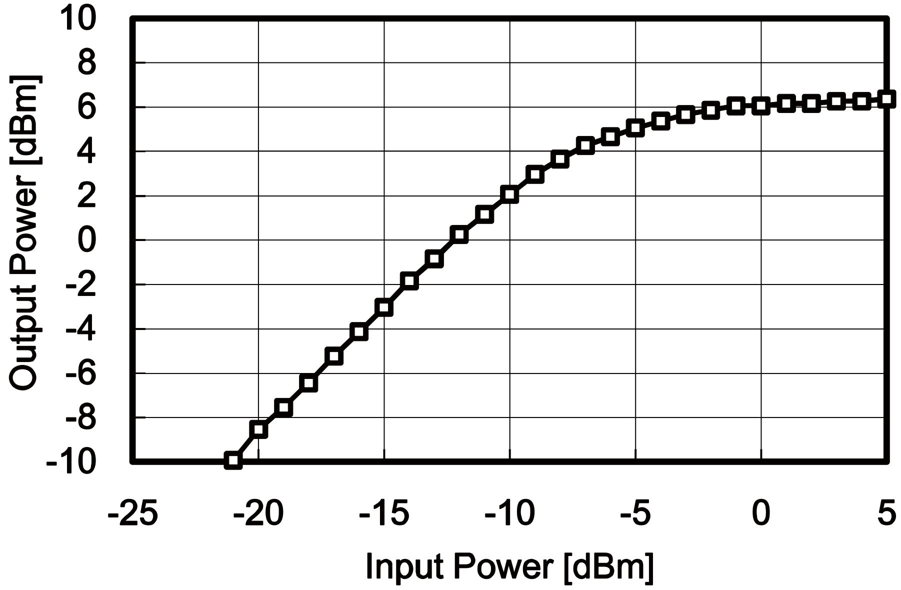
3-Stage PA

- **TL-based design for simulation accuracy**
- **Low-loss TL & MIM TL**



Tx Measurement





CG: 16dB

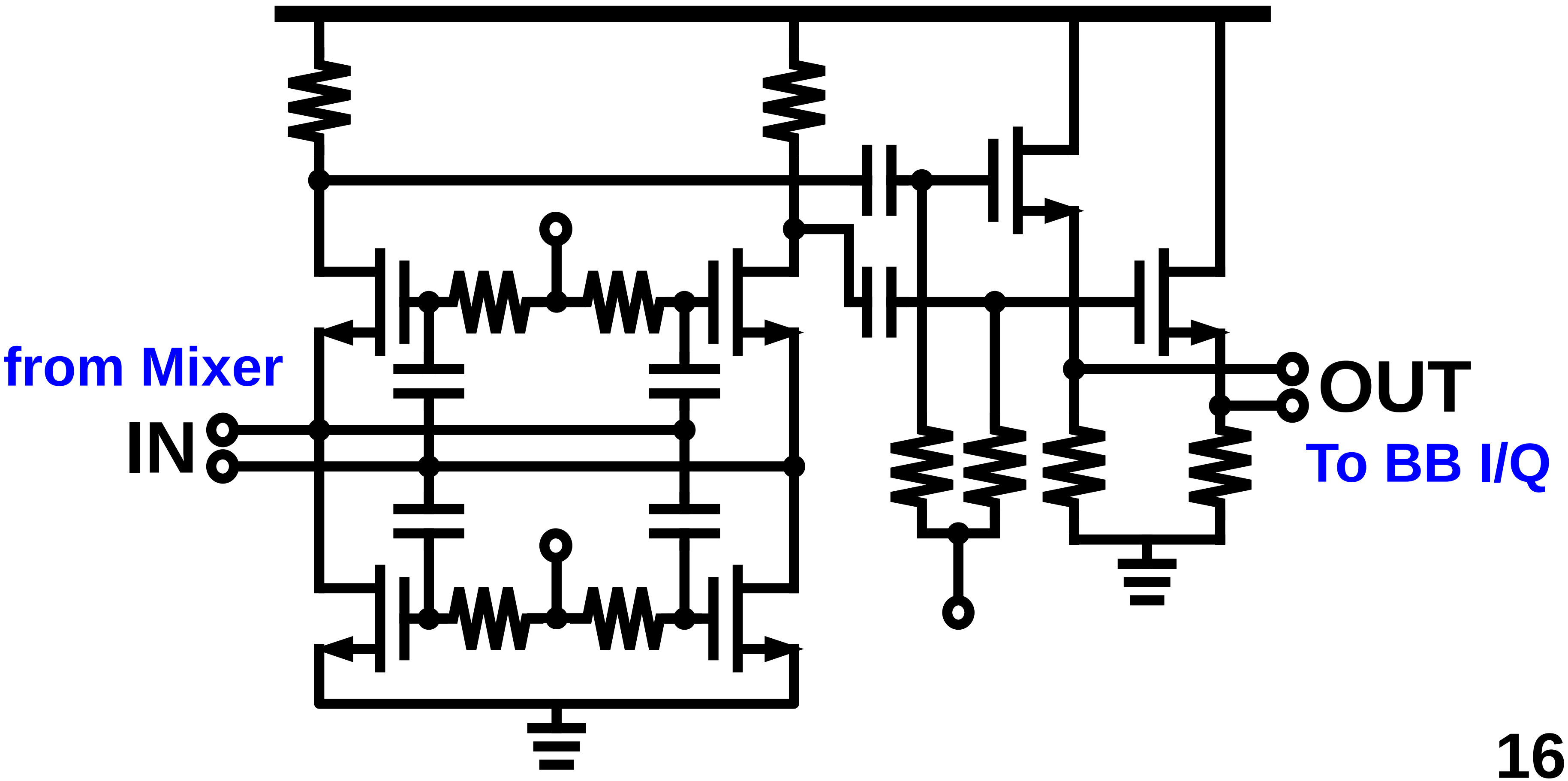
P_{DC}: 181mW

P_{sat}: 6.5dBm(ch2)

P_{1dB}: 5.4dBm(ch2)

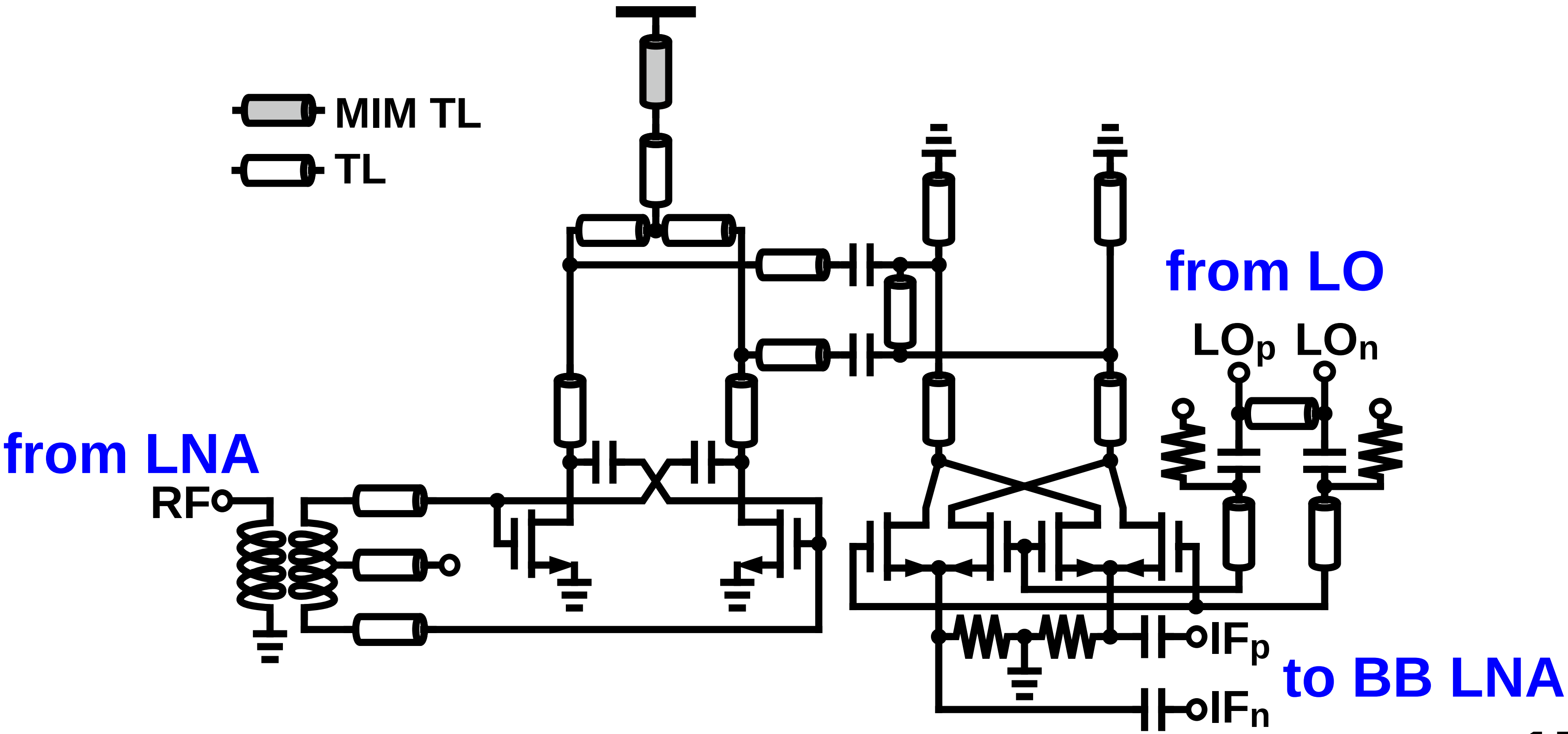
BB LNA

- CCC amplifier with a source-follower buffer.
- To compensate Noise Figure



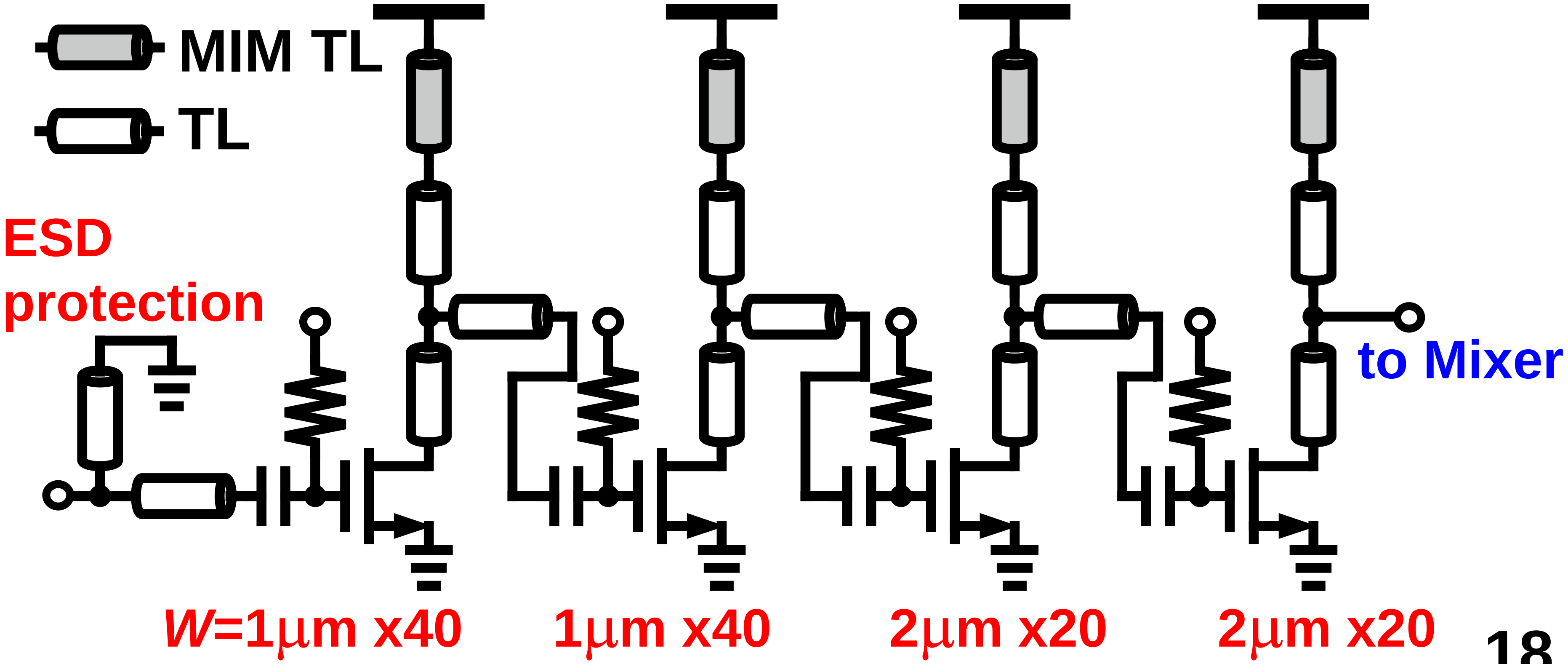
Down-Conversion Mixer

- Parallel-line transformer
- Capacitive cross-coupling neutralization

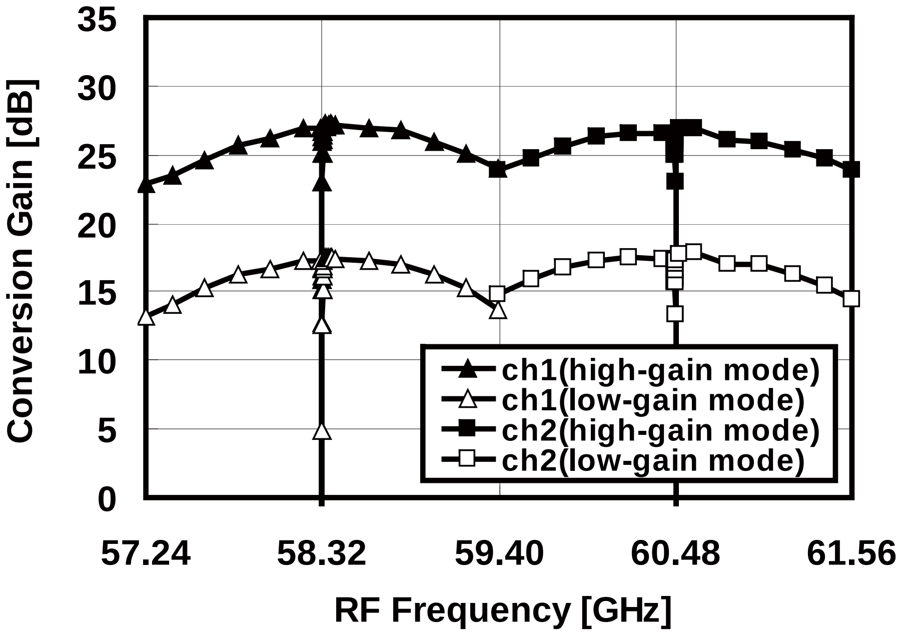


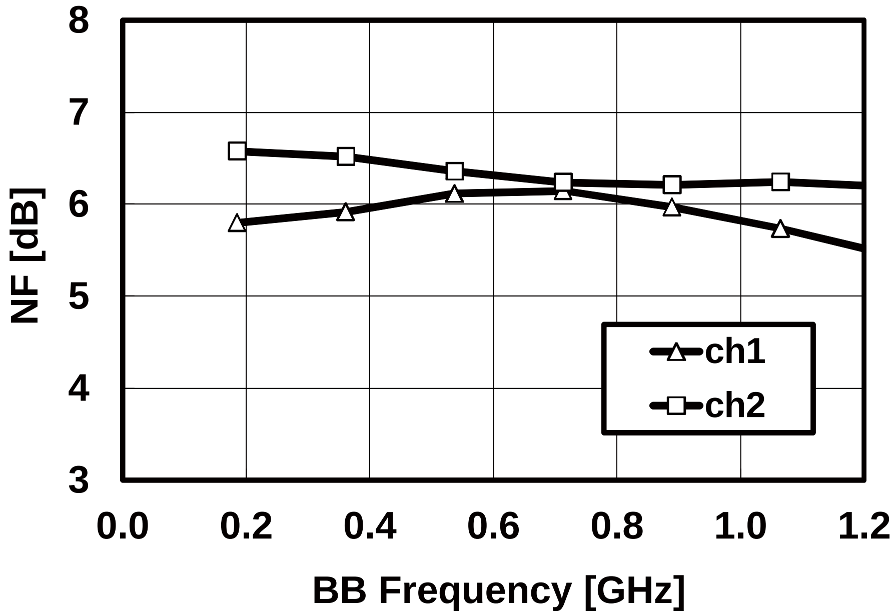
4-Stage CS-CS LNA

- W_f=1μm (1st & 2nd stages) for noise opt.
- W_f=2μm (3rd & 4th stages) for gain opt.
- Variable gain by adjusting bias voltages



Rx Measurement

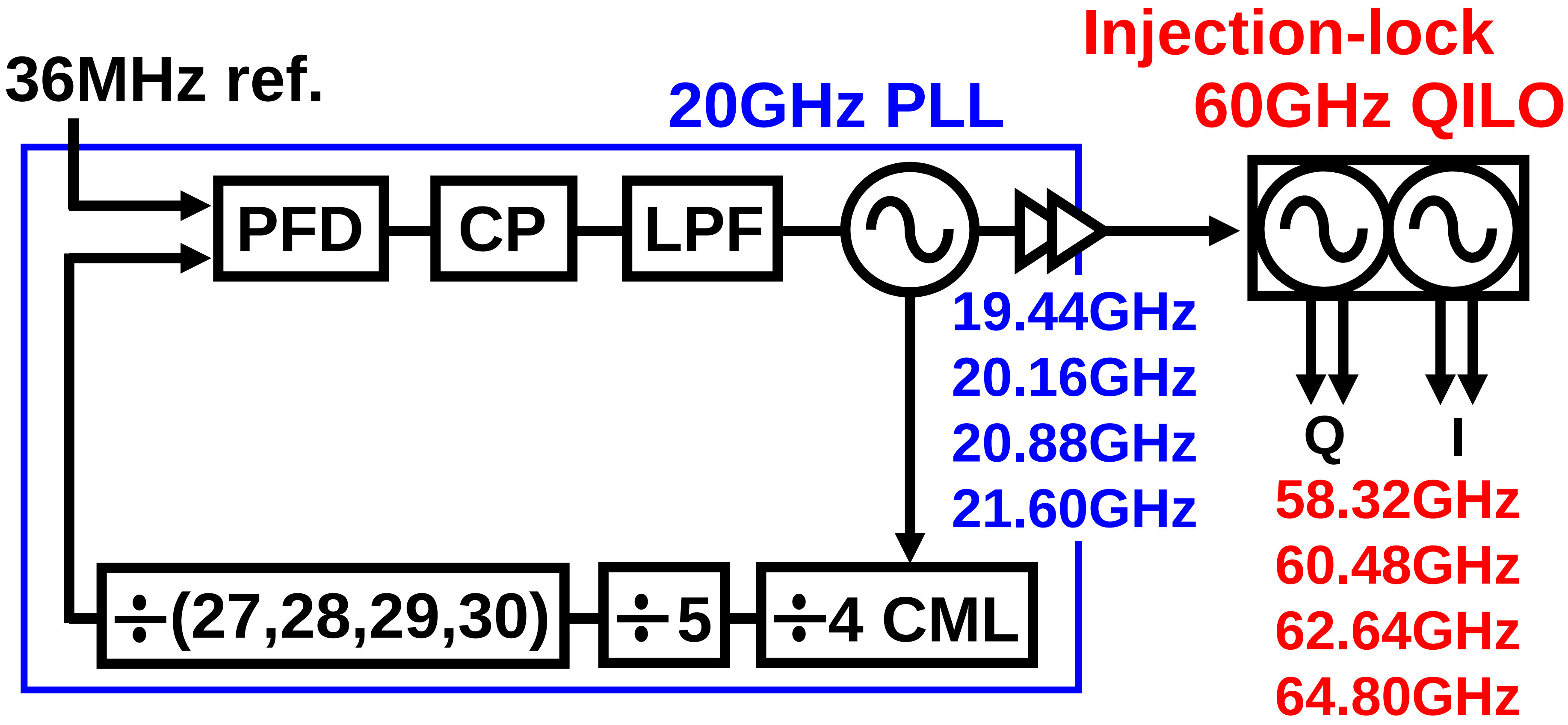




CG: 17-27dB
NF: <6.1dB (ch2)

LO freq.: 60.48GHz (ch2)
Lower cut-off freq.: 4MHz
P_{DC}: 138mW

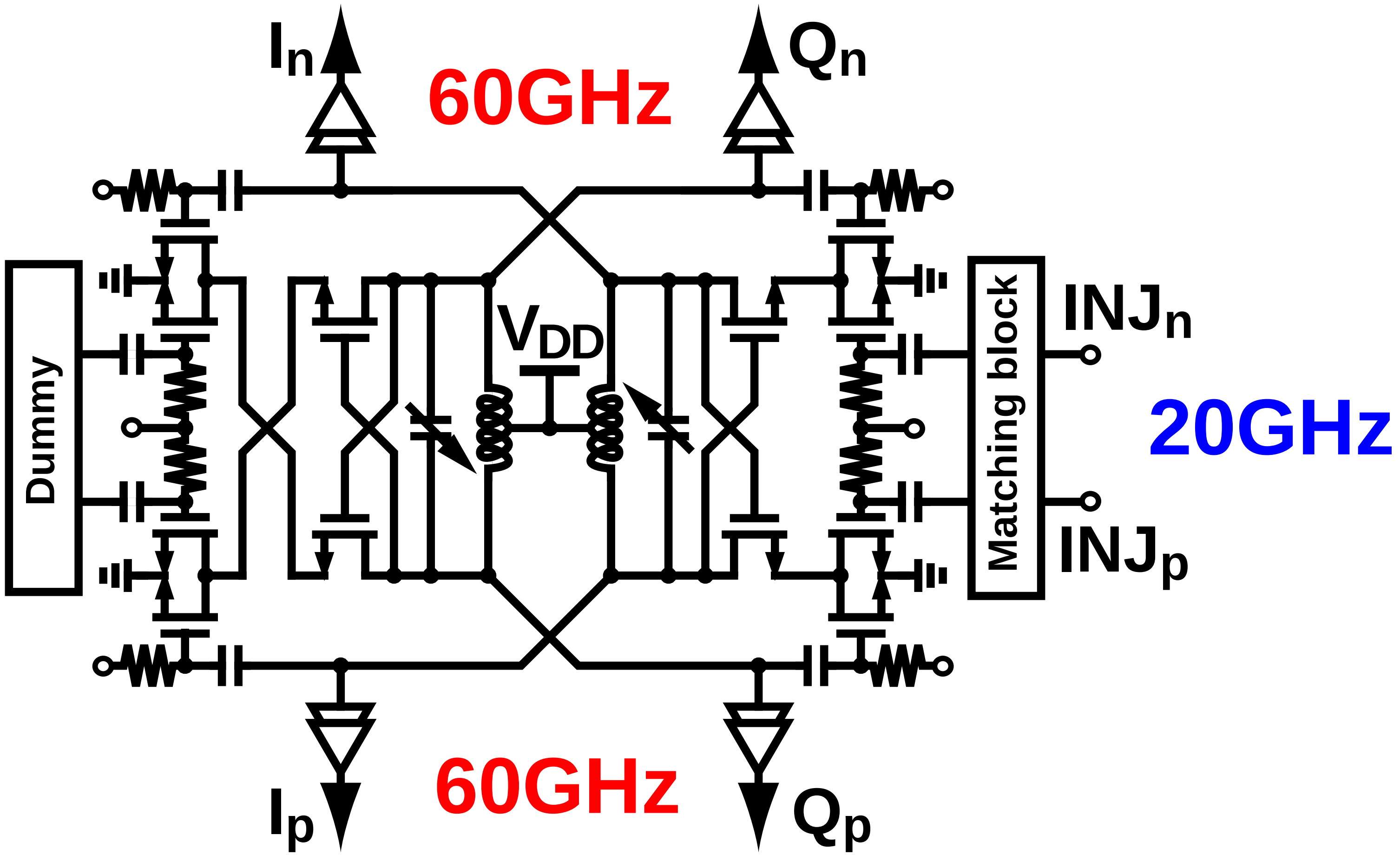
60GHz Quadrature LO



- Wide frequency tuning range
- Phase noise improvement by injection locking

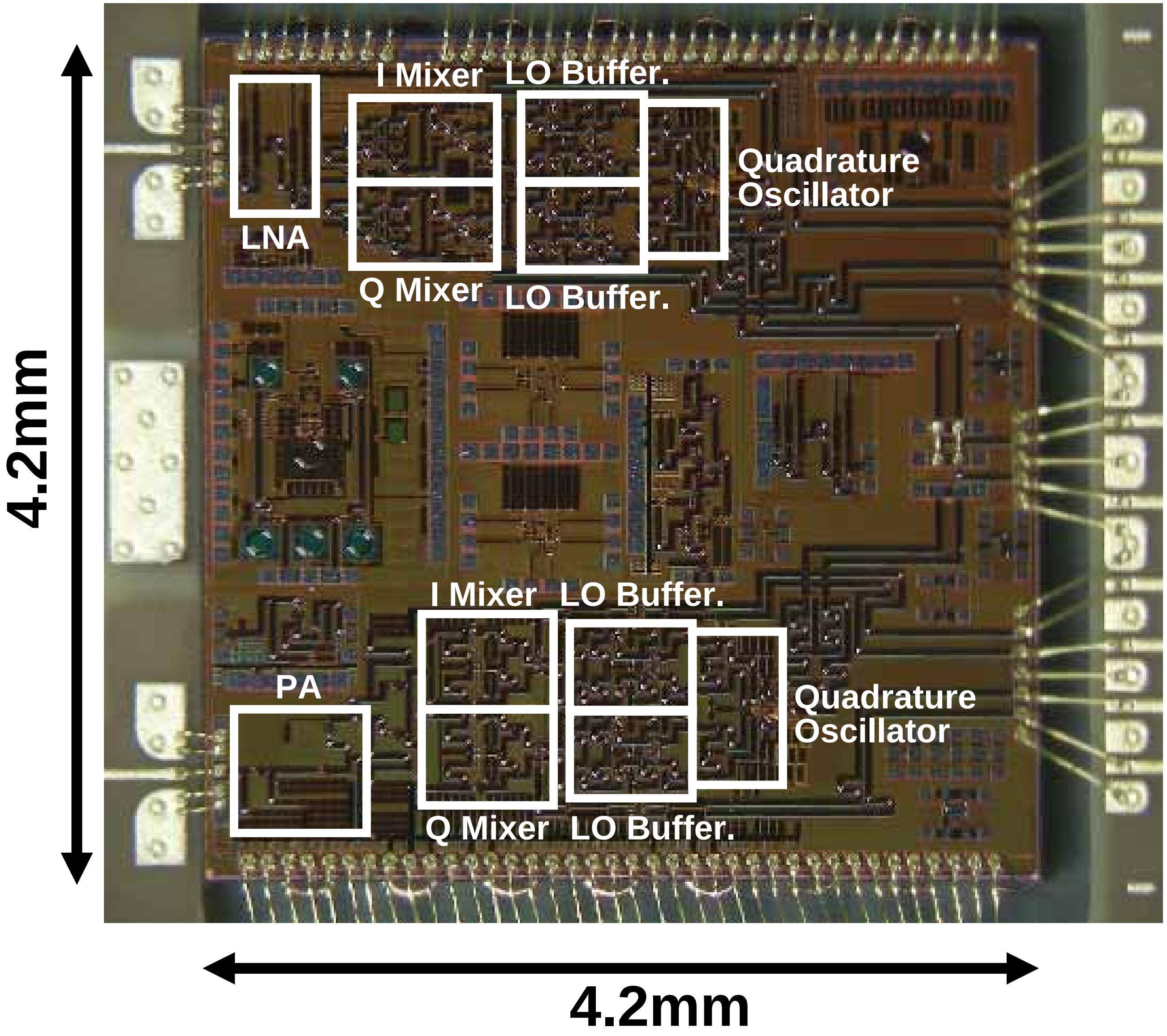
[4] A. Musa, *et al*., ASSCC 2010

Quadrature Injection-Locked Oscillator

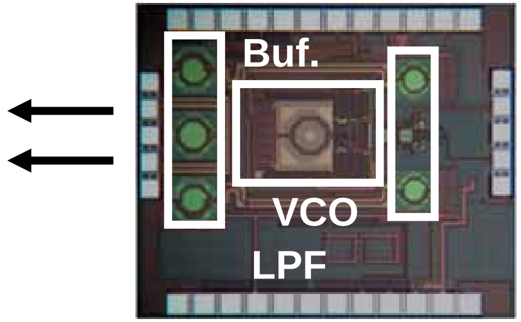


- Phase noise :-94.2dBc/Hz@1MHz-offset
- Free-running frequency: 55-63 GHz

Die Photo

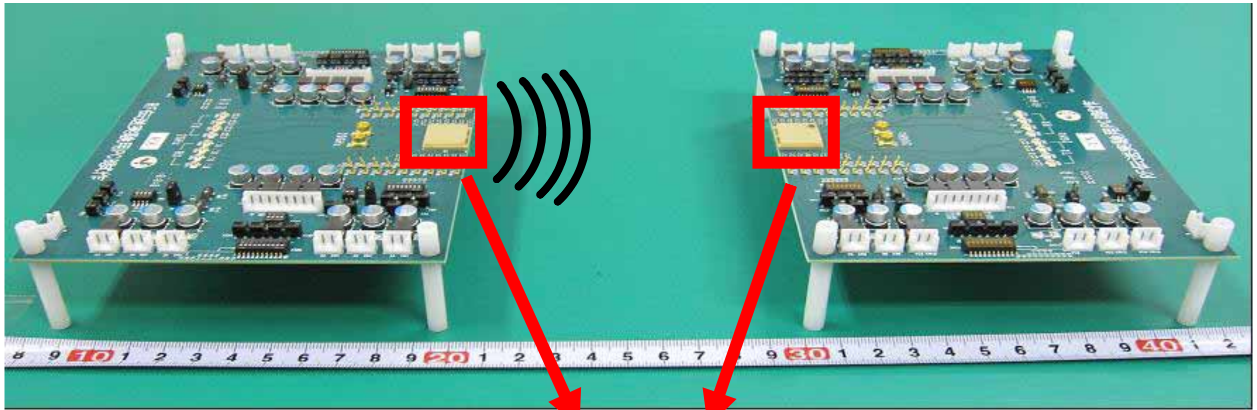


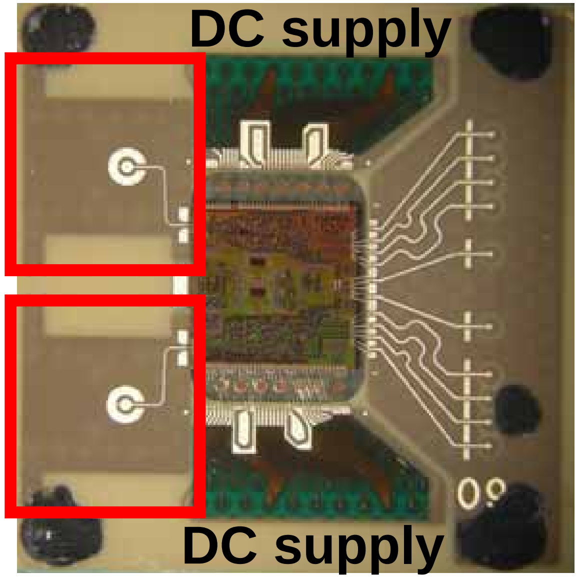
65nm CMOS
Rx:2.5mm²
Tx:2.3mm²
PLL:1.2mm²



20GHz PLL

Package and PCB





60GHz Rx
2dBi antenna

60GHz Tx
2dBi antenna

I/Q output (Rx)

20GHz PLL

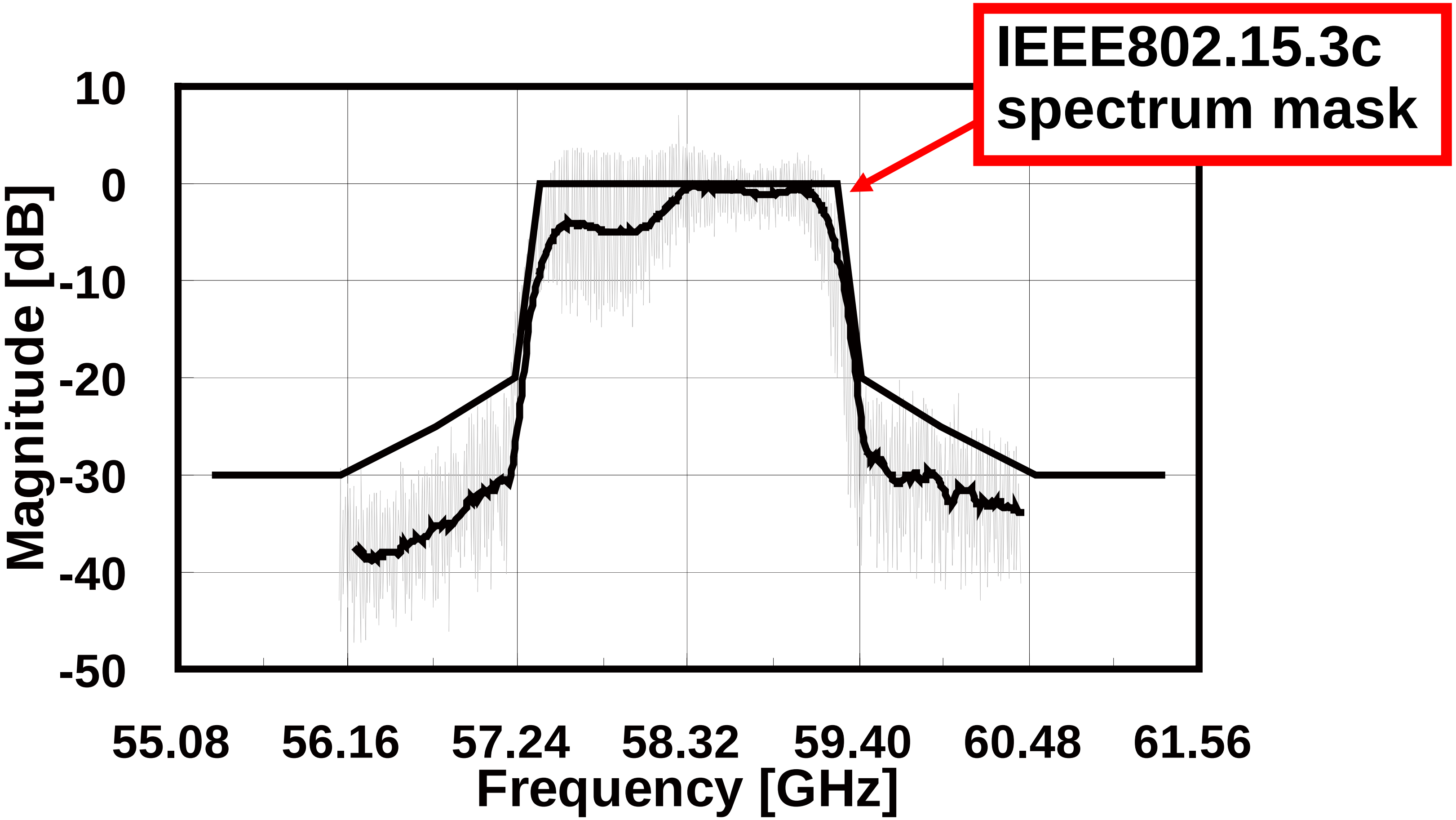
I/Q input (Tx)

Face-up mount with a 270μm wire on a BGA package

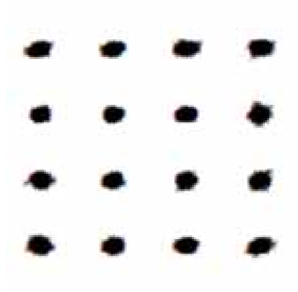
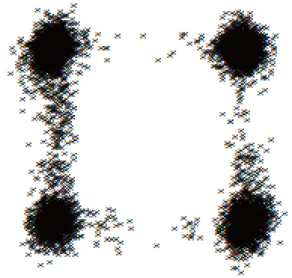
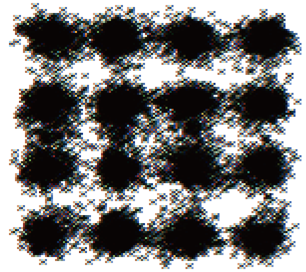
[5] R. Suga, *et al*., IEEE T-MTT 2010

Measured Spectrum

- **1.760Gs/s QPSK with 25% roll-off, 3dB back-off**



Modulation Characteristics

Constellation	 9506 points	 19912 points	 13502 points	 42024 points
Modulation	QPSK	16QAM	QPSK	16QAM
Data rate (BER $<10^{-3}$)	3.52Gb/s	7.04Gb/s	10.0Gb/s	16.0Gb/s
EVM (with DFE)	-30.5dB	-28.2dB	-15.2dB	-16.1dB

10Gb/s(QPSK) and 16Gb/s(16QAM) with wider-BW

Performance Comparison

	Data rate / Modulation	EVM	Direct conv.	Power
U. Toronto[6]	4Gb/s(BPSK)	N/A	Yes	374mW
UCB [1]	4Gb/s(QPSK) 7Gb/s(QPSK) (loop-back)	N/A	Yes	170mW(Tx mode) 138mW(Rx mode)
Tokyo Tech[2]	8Gb/s(QPSK) 11Gb/s(16QAM)	-17dB (Tx→Rx)	Yes	186mW(Tx mode) 106mW(Rx mode)
CEA-LETI[7]	3.8Gb/s(16QAM)	-20.7dB(Tx) -19.2dB(Rx)	No	1357mW(Tx mode) 454mW(Rx mode)
SiBeam[8]	3.8Gb/s(16QAM)	-19.2dB (Tx→Rx)	No	1820mW(Tx mode) 1250mW(Rx mode)
This work	10Gb/s(QPSK) 16Gb/s(16QAM)	-28.2dB (Tx→Rx)	Yes	181mW(Tx mode) 138mW(Rx mode)

[6] A. Tomkins, *et al.*, *JSSC*, vol.44, no.8, pp.2085-2099, Aug. 2009 [7] A. Siligaris, *et al.*, *ISSCC 2011.*, pp. 162-163 [8] S. Emami, *et al.*, *ISSCC 2011*, pp. 164-165

Summary and Conclusion

- A 60GHz 16Gb/s 16QAM Low-Power Direct-Conversion Transceiver.
- Consideration of mixer layout.
- Capacitive Cross-Coupling Neutralization.
- Full-rate 16QAM/8PSK/QPSK/BPSK for IEEE802.15.3c
- Ch1(57.24-59.40GHz) and Ch2(59.40-61.56GHz)
- Standard 65nm CMOS
- Tx (181mW), Rx (138mW), and PLL (66mW)