A 6-10 GHz Tunable Power Amplifier for Reconfigurable RF Transceivers

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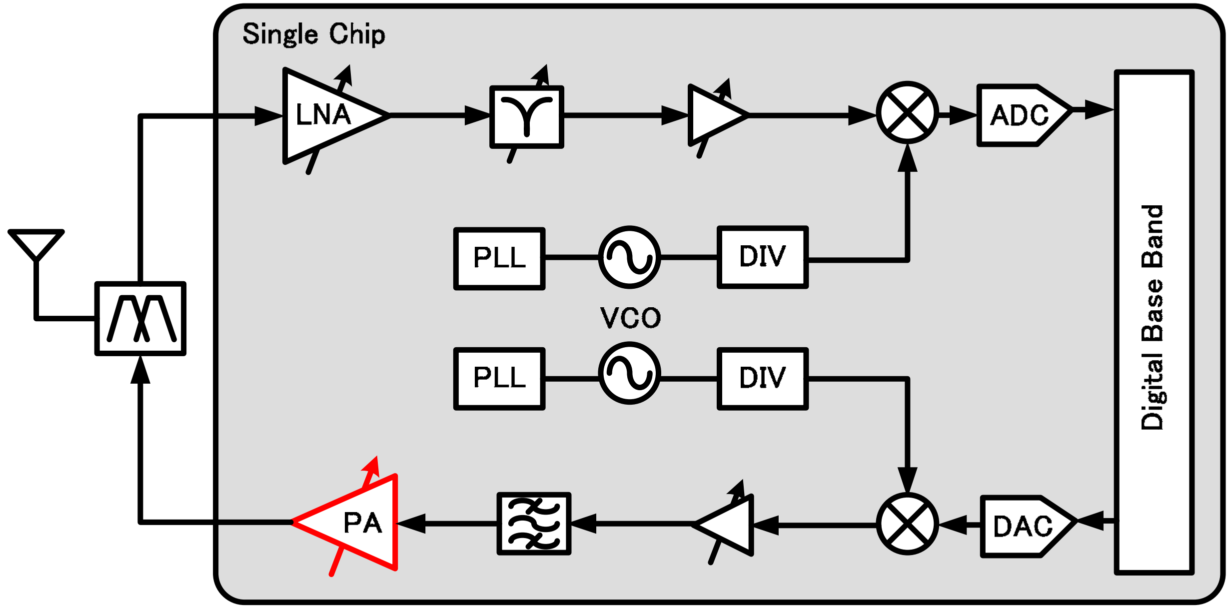
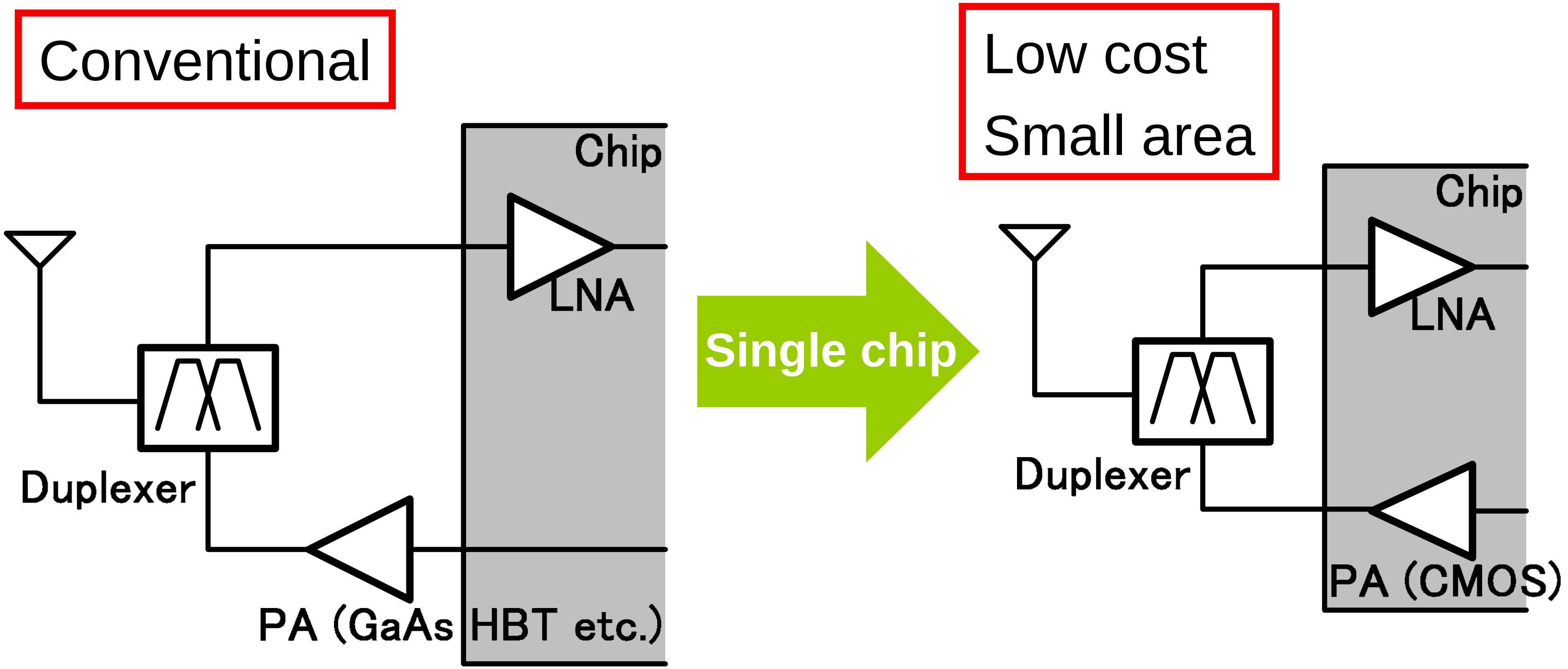
Introduction



- **PA (Power Amplifier)**

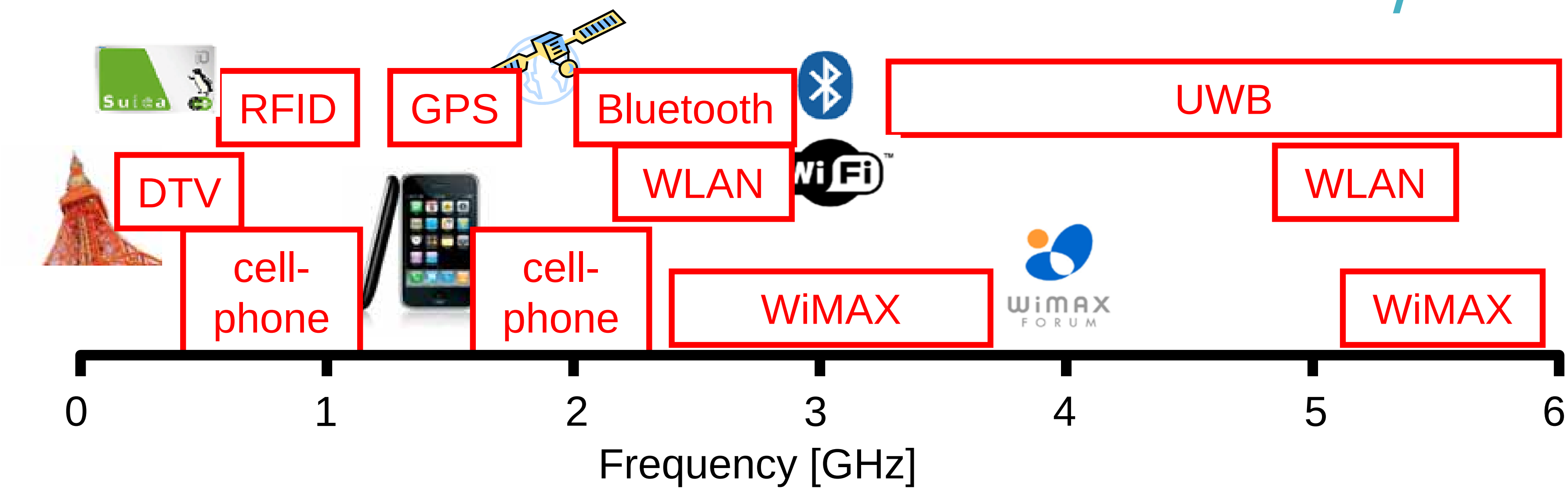
: A circuit used to convert a low-power RF signal into a larger signal of significant power at transmitter

Introduction



- **Single chip transceiver is demanded because of its low cost and downsizing.**

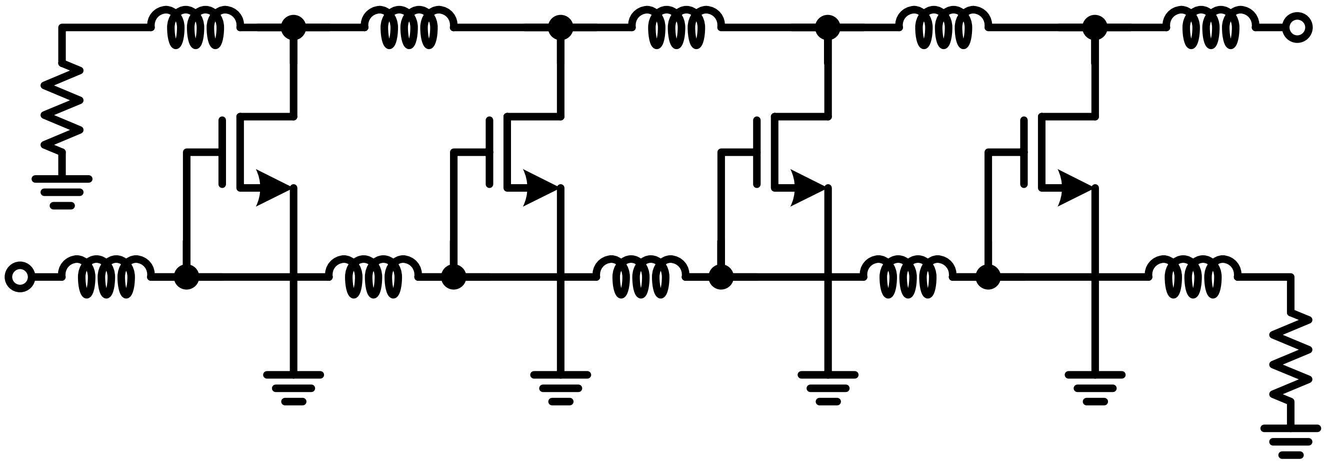
Introduction



- **Various wireless communication standards**
- **~ 6GHz : Various applications**
- **6~10GHz : Potential application**

Conventional wideband PA

- Distributed power amplifier

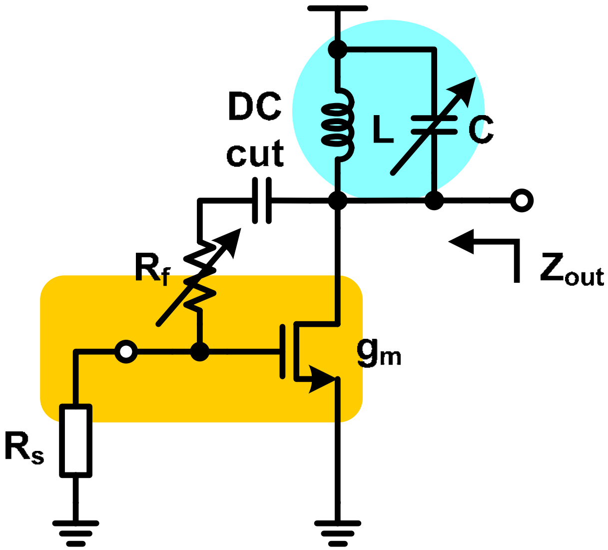


✓ **Wideband input / output matching**
→ Possibility of intermodulation

✗ **Lack of the optimum impedance matching**
→ Insufficient output power

✗ **Many inductor** → Large area

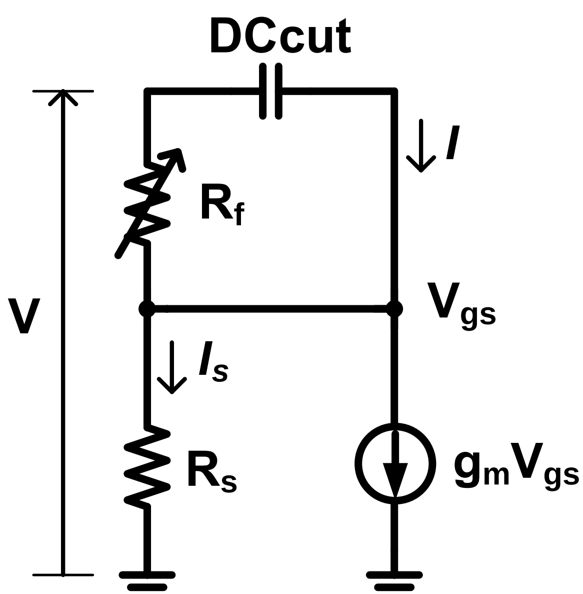
Output impedance matching



If $r_{ds}=\infty$,

$$Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} // \frac{1}{j\omega C} // (R_L + j\omega L)$$

※R_s: source impedance (50Ω)
※R_L: inductor parasitic resistance



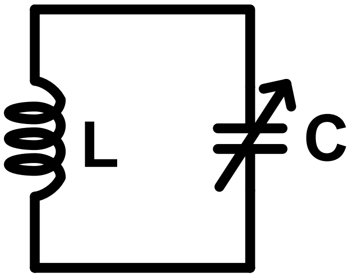
$$V = V_{gs} + \frac{V_{gs}}{R_s} R_f$$

$$I = I_s + g_m V_{gs} = \left(\frac{1}{R_s} + g_m\right) V_{gs}$$

$$\therefore Z = \frac{V}{I} = \frac{R_f + R_s}{g_m R_s + 1}$$

Output impedance matching

$$Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} // \frac{1}{j\omega C} //(R_L + j\omega L)$$



$$Z = \frac{1}{j\omega C} //(R_L + j\omega L)$$

$$= \frac{1}{\frac{1}{(R_L + j\omega L)} + j\omega C} = \frac{R_L + j\omega(L - R_L^2 C - \omega^2 L^2 C)}{(1-\omega^2 LC)^2 - \omega^2 R_L^2 C^2}$$

(Calculation of resonance frequency)

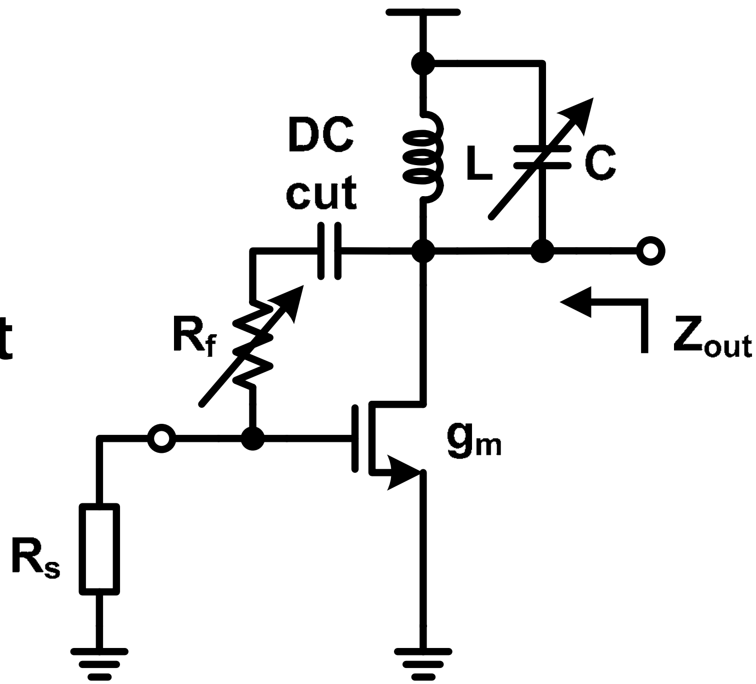
$$L - R_L^2 C - \omega^2 L^2 C = 0$$

When $\omega = \sqrt{\frac{1}{LC} - \left(\frac{R_L}{L}\right)^2}$, $Z = \frac{L}{R_L C}$

$$\therefore Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} // \frac{L}{CR_L}$$

Output impedance matching

$$Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} // \frac{L}{CR_L}$$



① Tune C
→ cancellation of an imaginary part

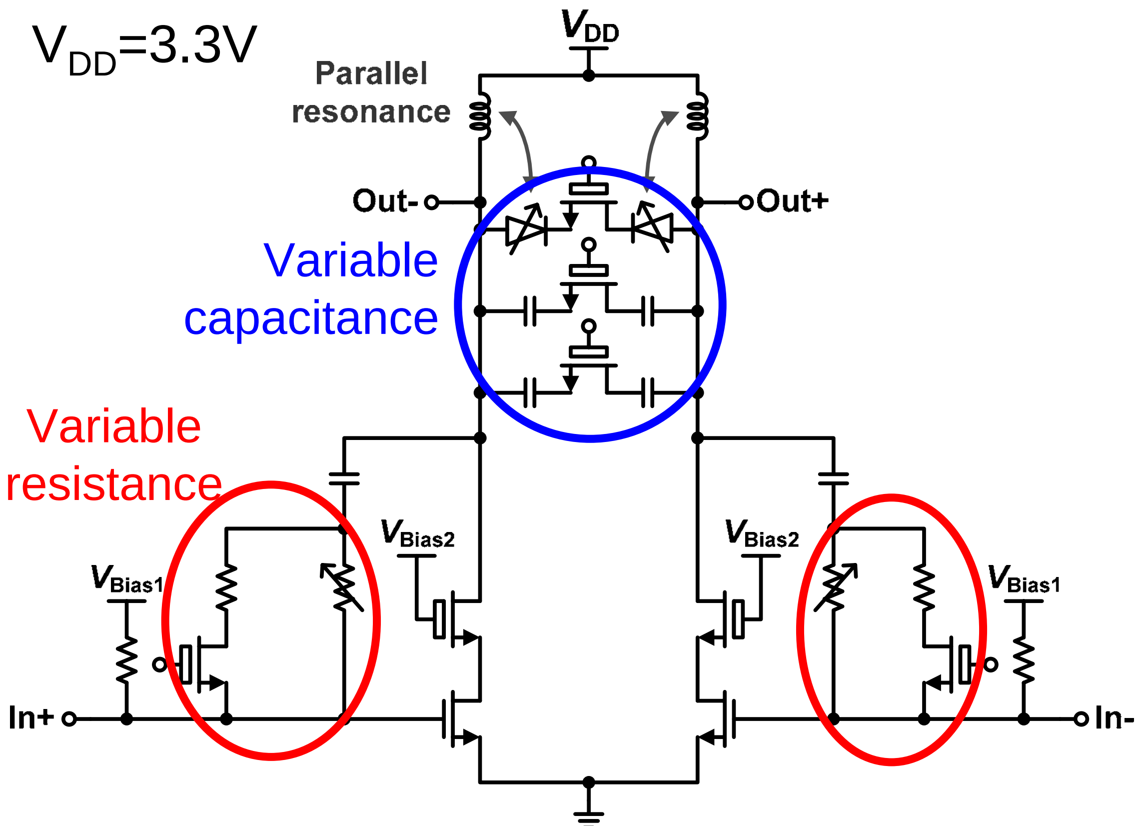
② Tune R_f
→ adjustment of a real part (50Ω)

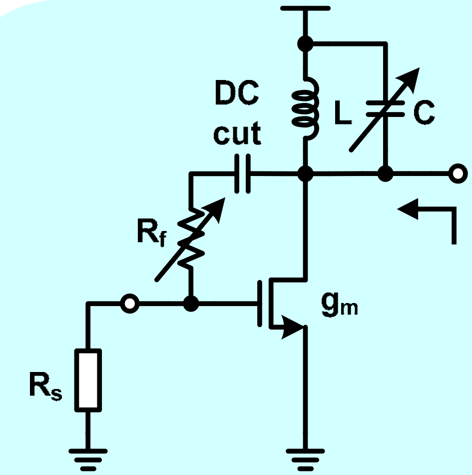
Z_{out} depends on resonance frequency

➡ Z_{out} can be matched 50Ω at arbitrary frequency

In fact, r_{ds} is small → Cascode topology raises r_{ds}

Schematic





R_s : source impedance (50Ω)

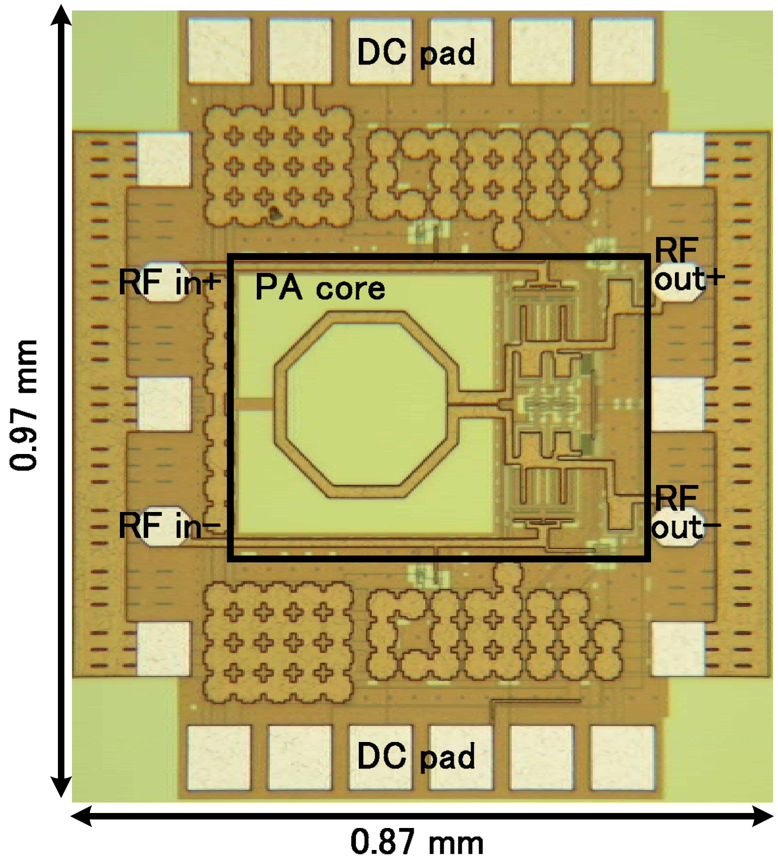
R_L : inductor parasitic resistance

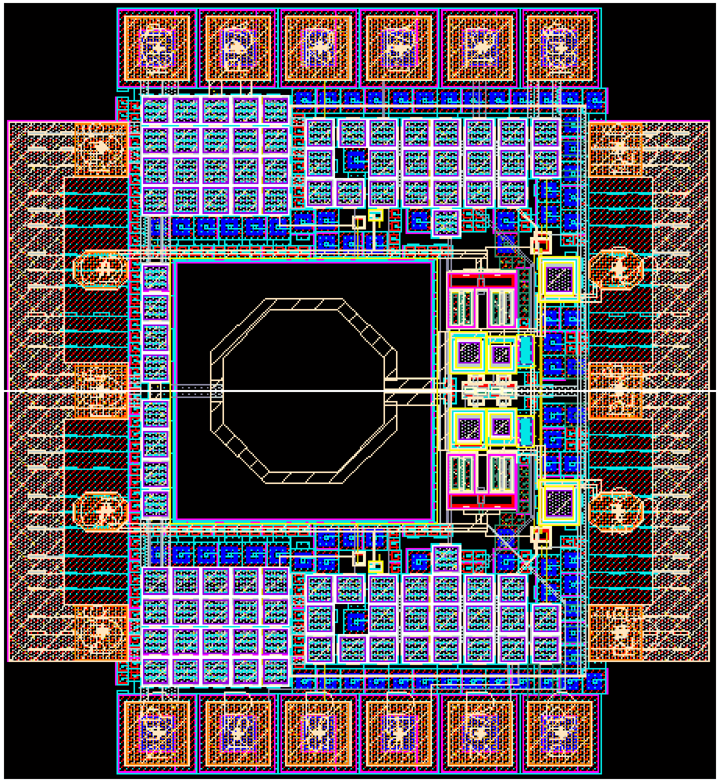
$$Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} // \frac{L}{CR_L}$$

- Class-A bias & Differential topology for 3dB larger P_{sat}
- Change output matching band by switching C and R
- Isolators was removed by maintaining Z_{out} to 50Ω

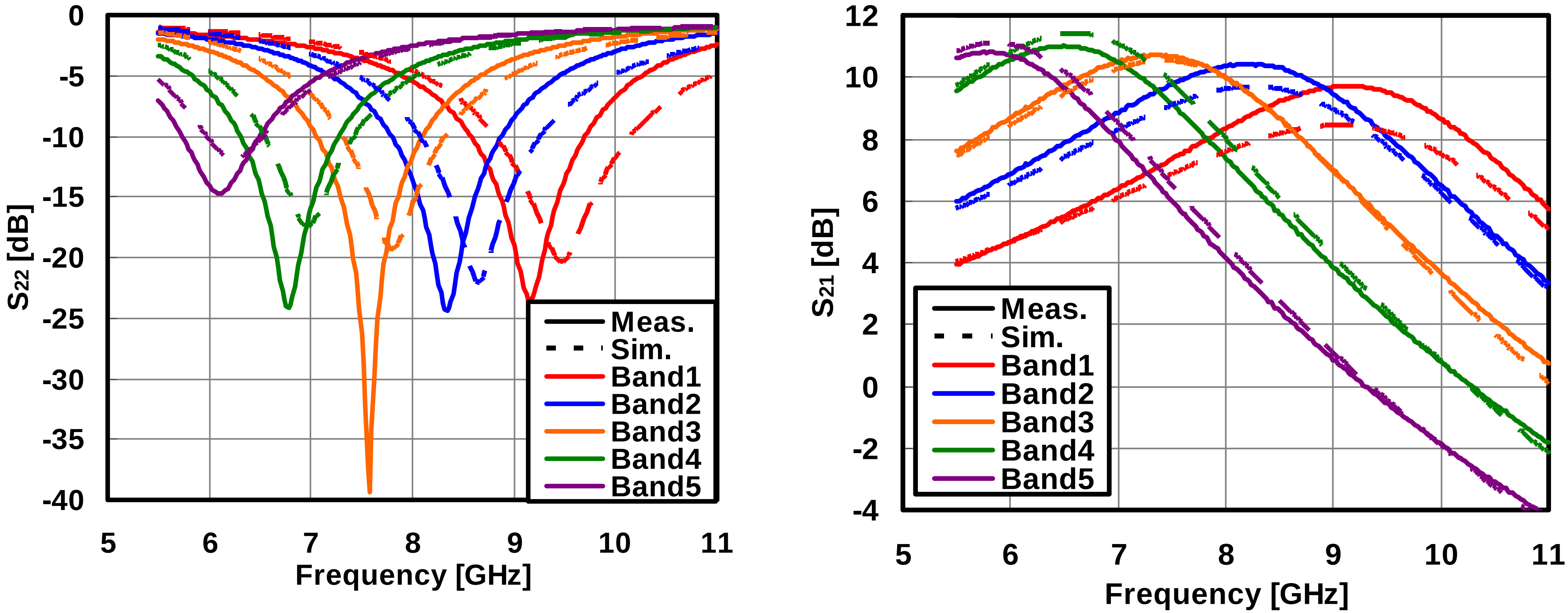
Chip micrograph

- **TSMC 0.18 μm CMOS process**





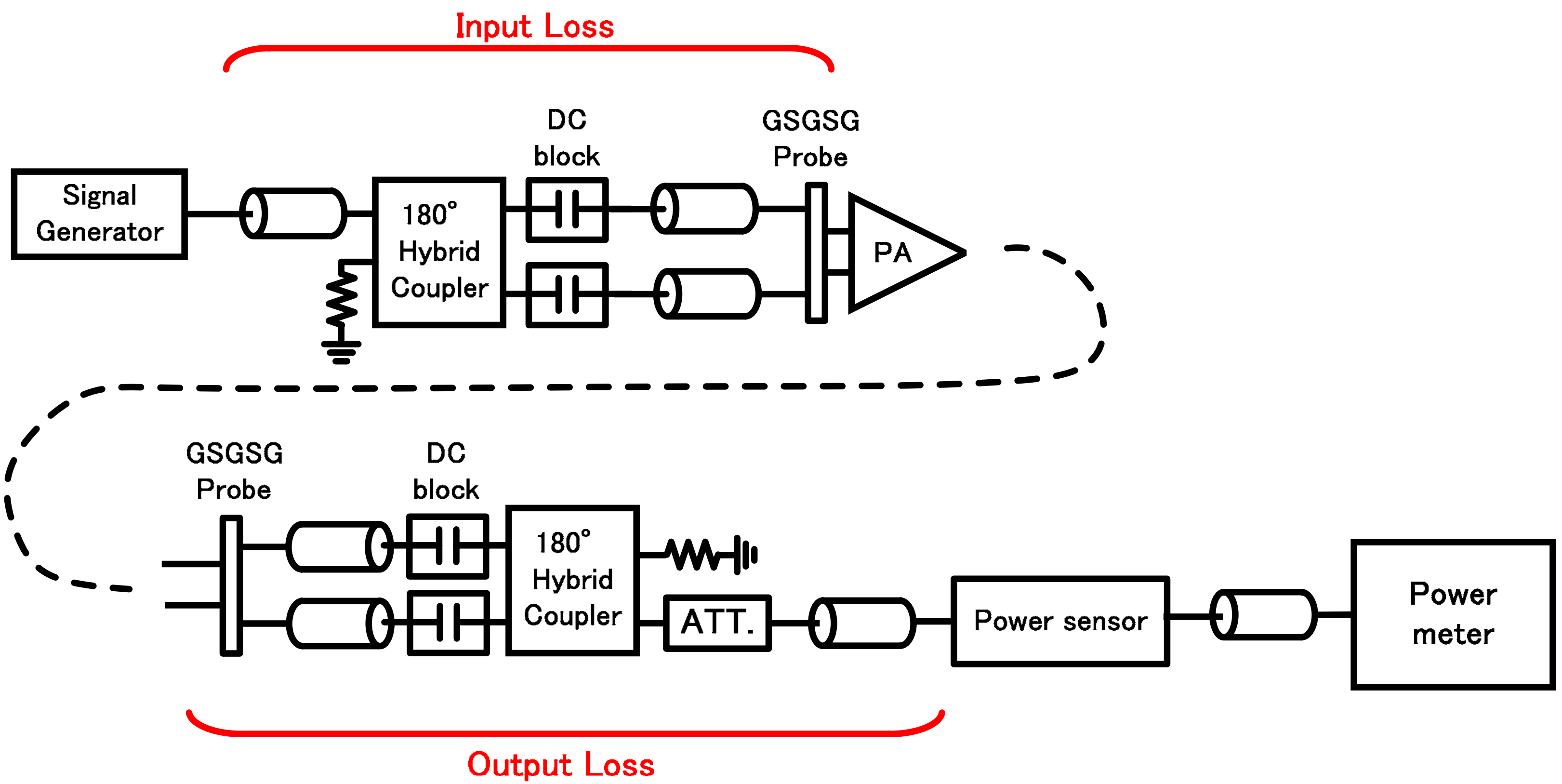
S-parameter measurement result



- **Measurement results are slightly shifted to lower frequency due to model inaccuracy**

Measuring system

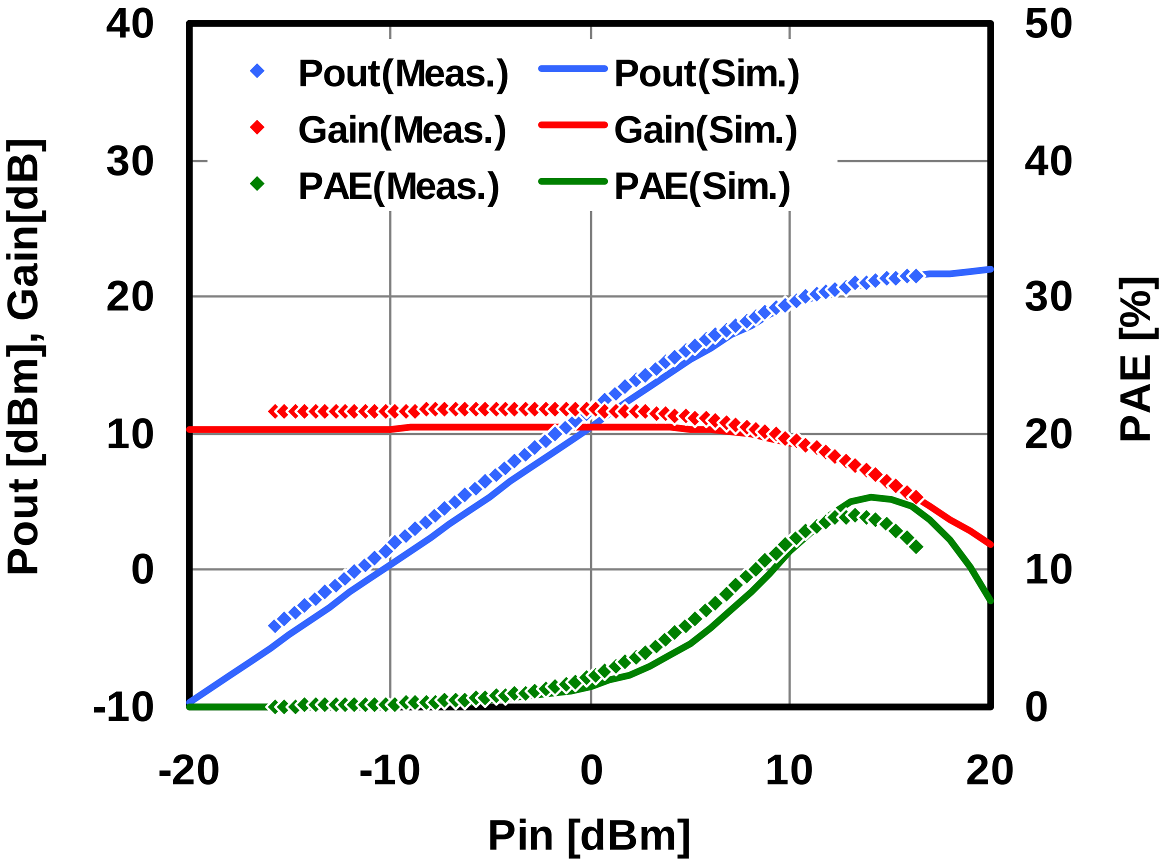
- Large signal measurement setup



- **Input and output losses are measured separately, and are calibrated from results.**

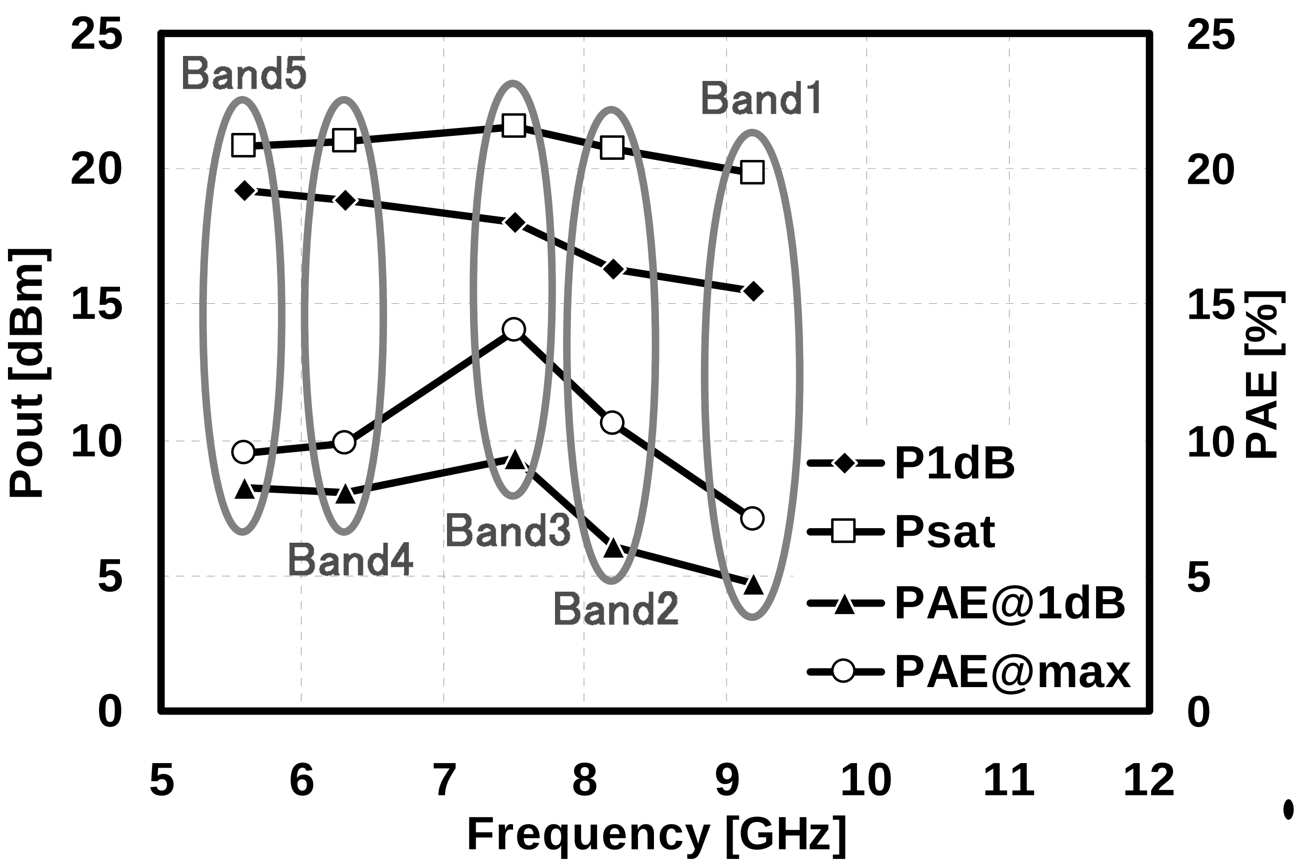
Large signal measurement result

- band 3 @ 7.5GHz



- Measurement and simulation results agree with each other.

Large signal measurement result



$$PAE = \frac{P_{out} - P_{in}}{P_{dc}}$$

- P_{1dB} > 15.5 dBm
- P_{sat} > 19.8 dBm
- PAE_{1dB} > 4.7%
- PAE_{max} > 7.1%

Summary

	Simulation	Measurement
Technology	TSMC 0.18 μm CMOS	
V_{DD}	3.3 V	
S_{22}	< -10 dB	
Frequency	6.0~10.2 GHz	5.7~9.7 GHz
P_{1dB}	17.6~19.4 dBm	16~19 dBm
P_{sat}	20.9~22.0 dBm	20~22 dBm
PAE_{peak}	9.7~15.3 %	7~14 %
Area	Core size：0.50×0.39 0.20 mm^2	

Comparison of CMOS PAs

	[1]	[2]	[3]	[4]	This work
Technology	0.09 μm	0.18 μm CMOS process			
V_{DD} [V]	-	1.5	2.0	-	3.3
Frequency [GHz]	*5.2~13	6~10	3~10	3.7~8.8	**5.74〜9.68**
P_{1dB} [dBm]	-	**5	5.6~9.4	~15.6	**15.5〜19.2**
P_{sat} [dBm]	25.2	-	-	19	19.8〜21.6
PAE_{peak} [%]	21.6	17.6	-	25	7.1~14.0
Area [mm²]	***0.70	1.08	1.76	2.8	***0.20

* S_{22}<-3dB ** Average P_{1dB} *** Core size

[1] H. Wang, et al., “A 5.2-to-13GHz Class-AB CMOS Power Amplifier with a 25.2dBm Peak Output Power at 21.6% PAE,” IEEE International Solid-State Circuits Conference, pp. 44-46, 2010

[2] H. Chung, et al., “A 6-10-GHz CMOS Power Amplifier with an Inter-stage Wideband Impedance Transformer for UWB Transmitters,” EuMC, pp. 305-308, Oct. 2008

[3] C. Lu, et al., “A CMOS Power Amplifier for Full-Band UWB Transmitters,” RFIC, pp. 397-400, June. 2006

[4] C. Lu, et al., “Linearization of CMOS Broadband Power Amplifiers Through Combined Multigated Transistors and Capacitance Compensation,” TMTT, pp. 2320-2328, Nov. 2007

Conclusion

- 6-10 GHz Multi-band tunable CMOS PA
  - For realization of single chip transceiver
  - To cover various standards
- Prototype of a CMOS PA
  - TSMC 0.18μm CMOS process
  - Using parallel resonance and resistive feedback
- Results
  - Frequency: 5.7 ~ 9.7 GHz
  - P_{1dB}>15.5 dBm, PAE_{peak}> 7.1%, Core size=0.20mm^2
  - **The first tunable CMOS PA at 6-10GHz**

Thank you for your attention.