

# Reconfigurable RF CMOS Circuits for Cognitive Radios

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**TOKYO TECH**  
*Pursuing Excellence*

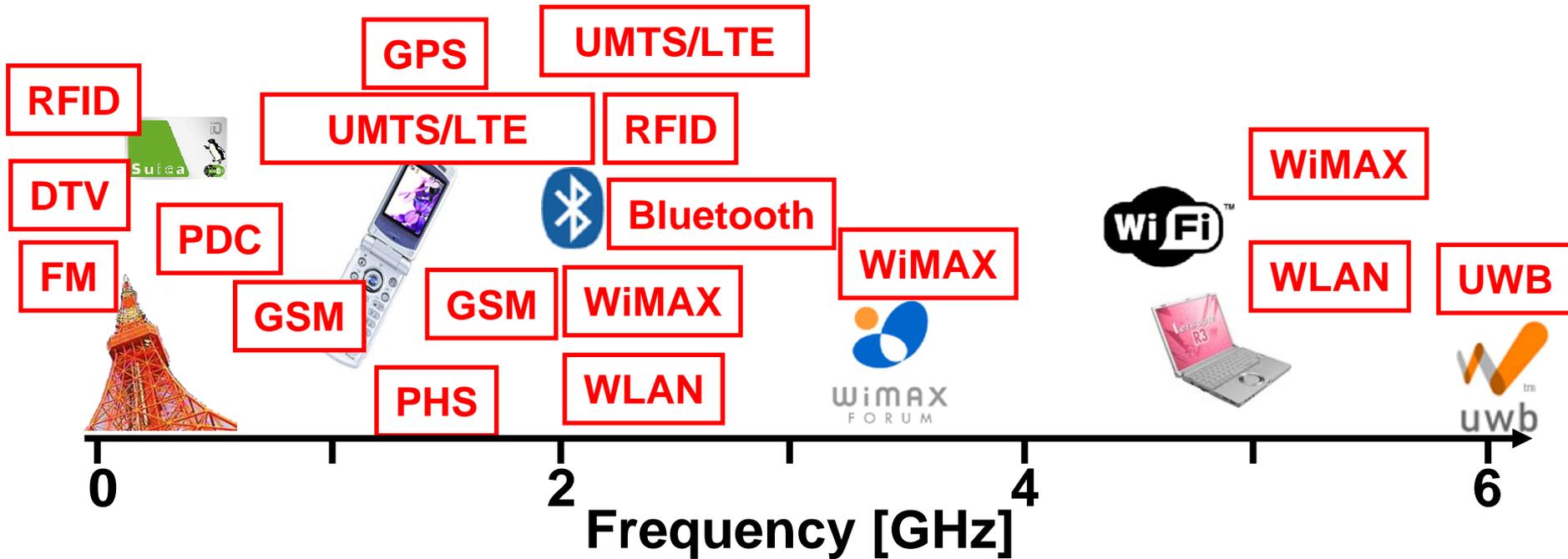


# Outline

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- **Roadmap for multi-standard RFIC**
- **Rx requirements**
  - **Linearity & NF**
- **LO requirements**
  - **Q and  $V_{DD}$**
  - **Frequency tuning range**
  - **Multiband VCO results**
- **Tx requirements**
  - **Tunable PA results**
- **Conclusion**

# Motivation



## Demand for a multi-standard RFIC

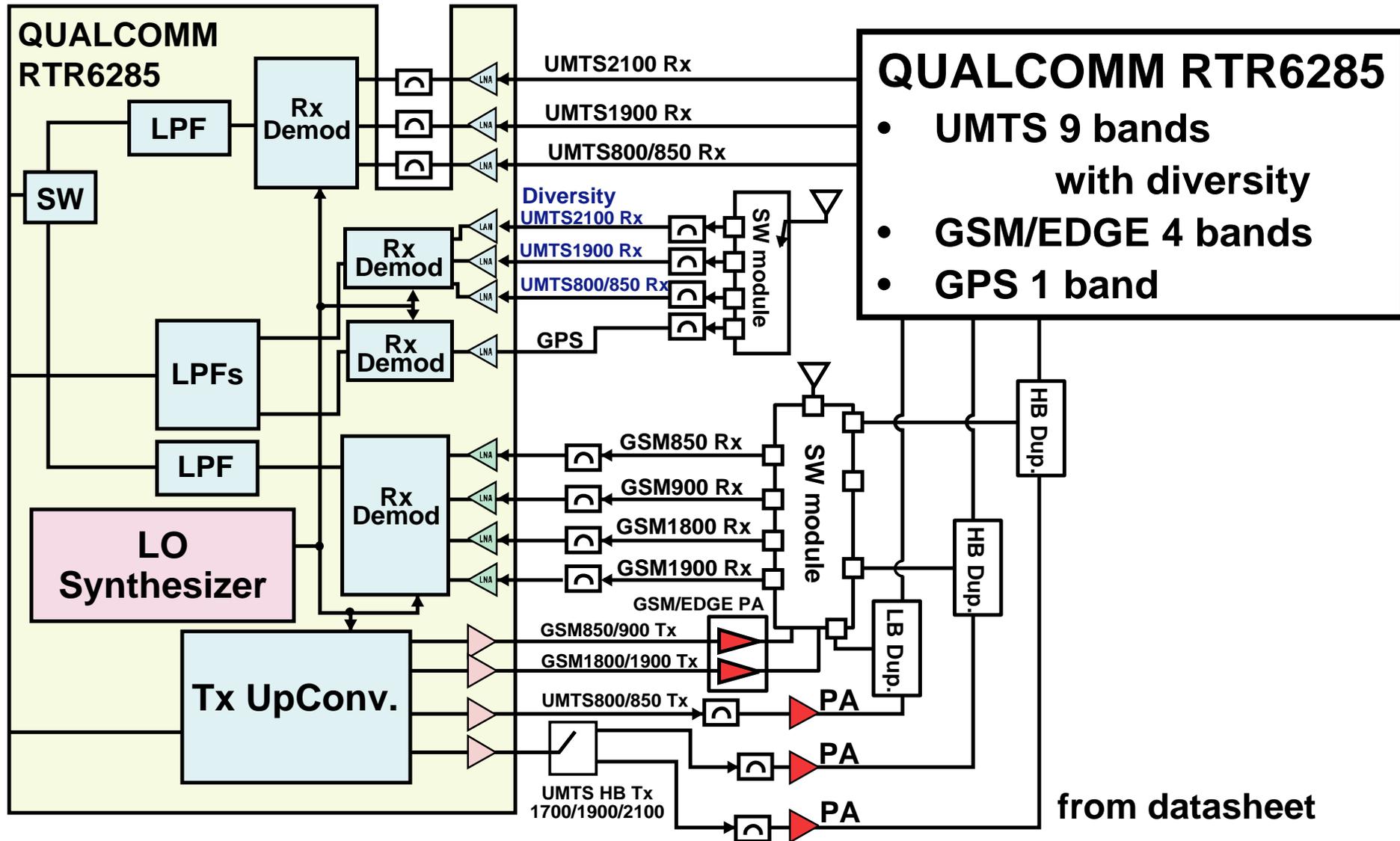
- Frequency range from 400MHz to 6GHz
- Smaller footprint
- Smaller number of components  
with competitive sensitivity and Pdc

# Multi-standard radio roadmap

		Present			Future
		individual approach	near-band combined	one-chip limited reconfiguration	one-chip full reconfiguration
Rx	LNA*	NF <2.2dB (2.5dB total)	NF <2.2dB (2.5dB total)	400MHz-6GHz NF <2dB	400MHz-6GHz NF <2dB
	Mixer	IIP3 >-5dBm	IIP3 >0dBm w/o SAW filter	IIP3 >0dBm w/o SAW filter	IIP3 >0dBm with tunable BPF/BRF
		IIP2 >40dBm	IIP2 >60dBm	IIP2 >70dBm	IIP2 >70dBm
Tx	PA	Off-chip PAs	Reduced off-chip PAs, Reduced off-chip matching	On-chip single-band PAs	On-chip multi-standard PA
			Off-chip multi-standard PAs	Off-chip multi-standard PA	
LO	VCO	GSM	GSM	-185dBc/Hz(FoM) no spurs, GSM	-190dBc/Hz(FoM) no spurs, GSM
		Multiple PLLs	Reduced multiple PLLs	400MHz-6GHz with 1 inductor	400MHz-6GHz with 1 inductor

\*Lower NF/sensitivity is required for some commercial applications.

# The present multi-standard RFIC

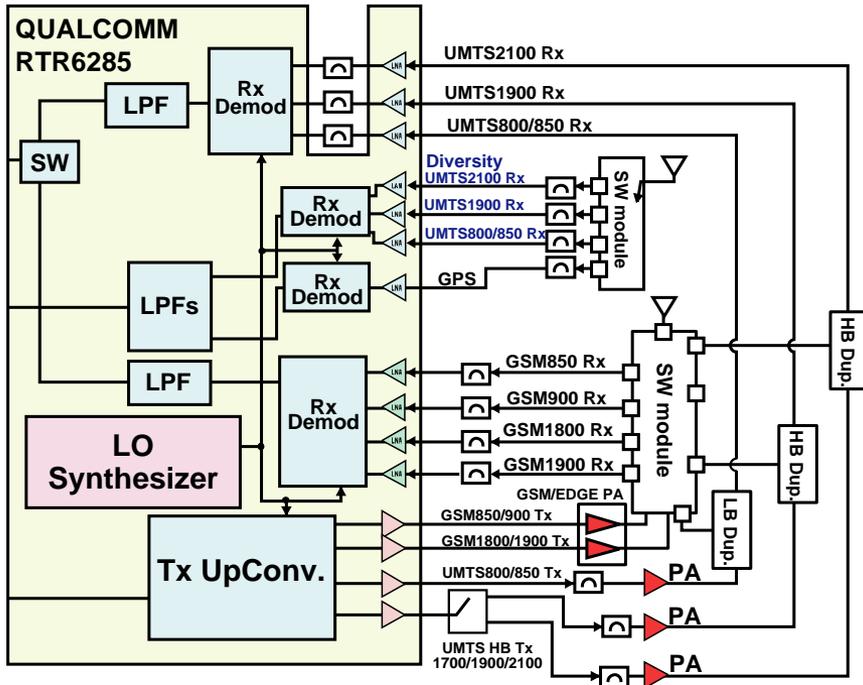


from datasheet

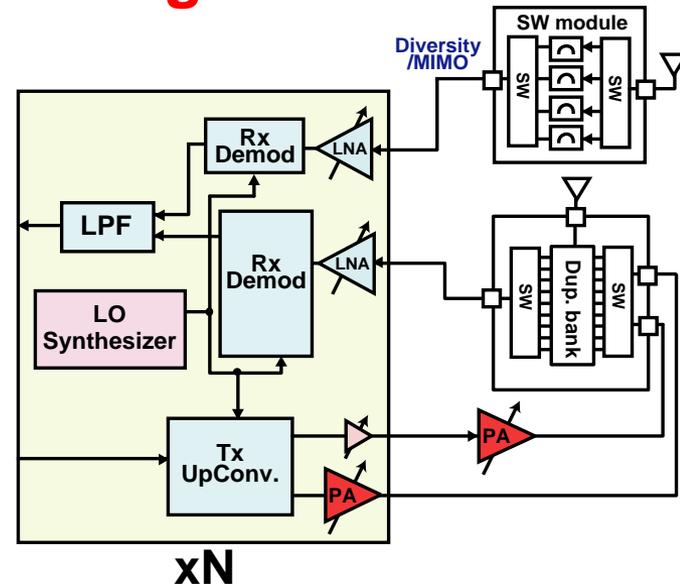
# The near-future multi-standard RFIC

- **Smaller number of IO pins and external components**
  - A single-ended input is better.
- **HB Rx(1.8-2.1GHz) should be combined without SAW filters.**
  - $NF < 2.2\text{dB}$ ,  $IIP3 > -2.5\text{dBm}$ ,  $IIP2 > 70\text{dBm}$**
- **GSM bands should also be combined.**
- **Handling of UMTS/LTE bands 7 and 11**
- **Must keep the same sensitivity with smaller area and smaller power consumption**

# One-chip Reconfigurable RFIC



## Reconfigurable RF front-end



- All cellular, WLAN/WPAN, and broadcast services should be covered.
- On-chip tunable Tx/Rx filters optimized for some particular bands
- On/off-chip tunable/switchable multi-standard PA
- External switchable duplexers are utilized for each FDD standard.

# One-chip full Reconfigurable RFIC

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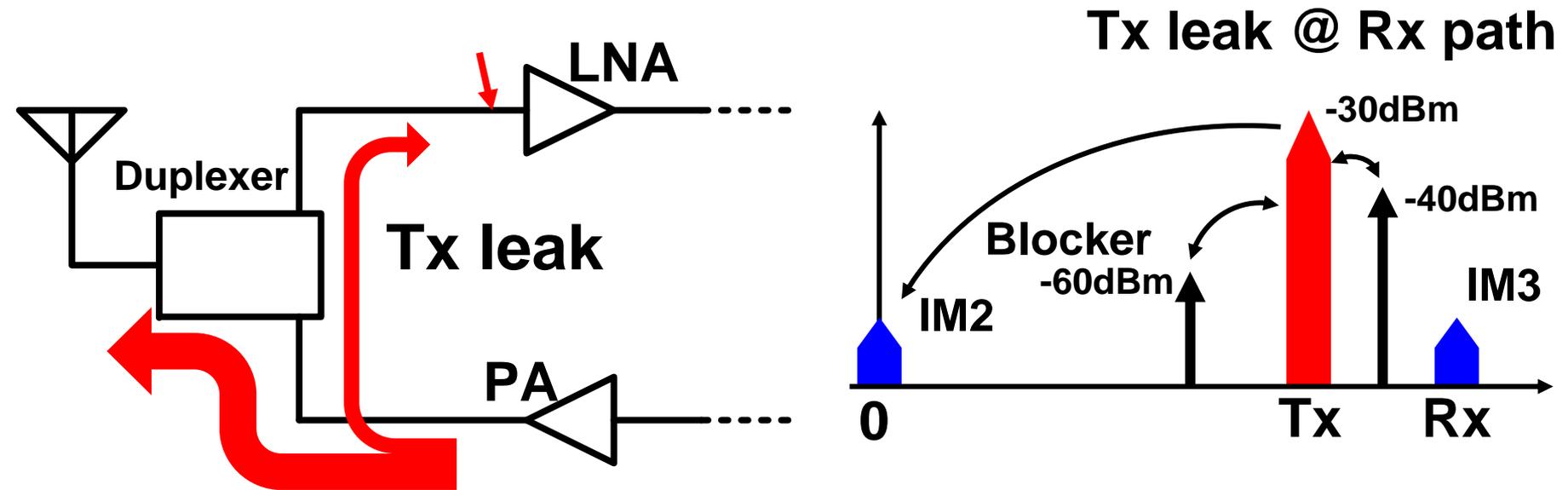
- **Equally designed for every bands**
- **Just advancement of NF and linearity improvement with tunable on-chip filters for possible interferers**
- **On/off-chip tunable/switchable multi-standard PA**
- **without special optimization for particular bands**
- **Possibly, external switchable duplexer/SW are still required.**
- **Seamless TDD/FDD reconfiguration**
- **Reconfigurability is required for RF/ABB**
- **Much smaller frequency step**
- **Cognition time (RF assisted)**

# Outline

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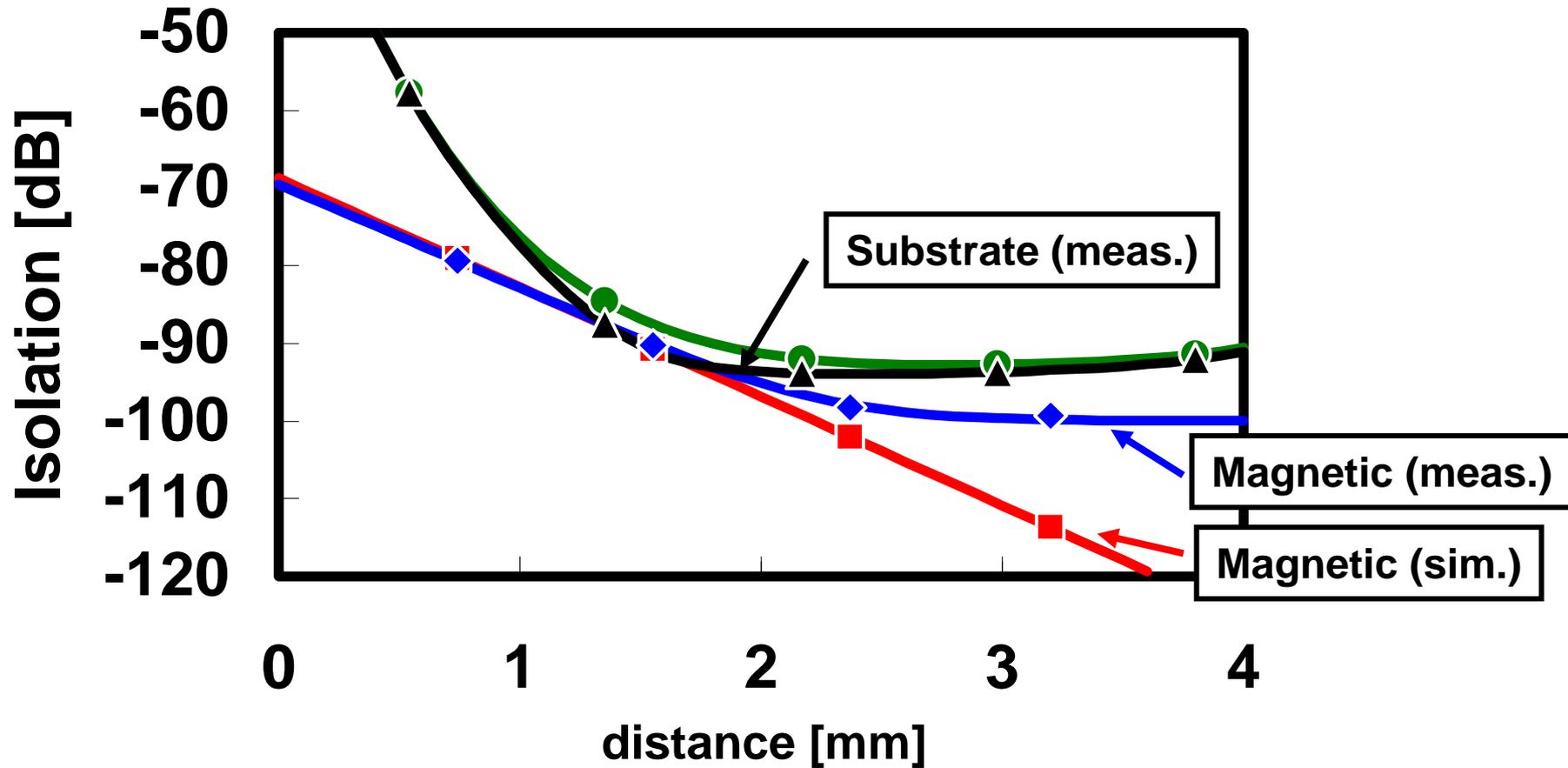
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# Rx requirements



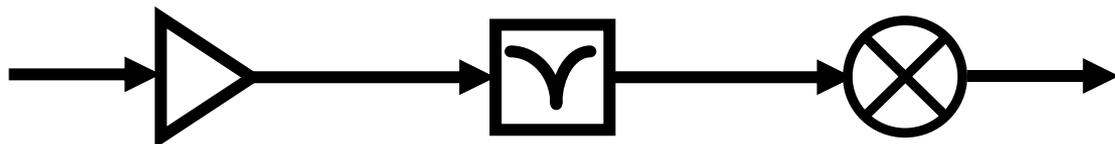
- **Linearity is very important for FDD systems like UMTS.**
- **Tx signal leaks into Rx path, and it becomes a very large interferer.**
- **Linearity is also very important, especially for concurrent operation of multiple on-chip transceivers.**

# On-Chip PA-to-LNA isolation



**Must consider isolation between on-chip RF blocks for concurrent operation of multiple front-ends**

# Requirements for SAW-less UMTS Rx



PG=15dB  
NF=2.2dB  
IIP3=0dBm

-20dB@Tx

PG=10dB  
NF=6dB  
IIP3=6.1dBm  
IIP2=30dBm



PG=15dB  
NF=2.2dB  
IIP3=0dBm

PG=10dB  
NF=6dB  
IIP3=16.1dBm  
IIP2=70dBm

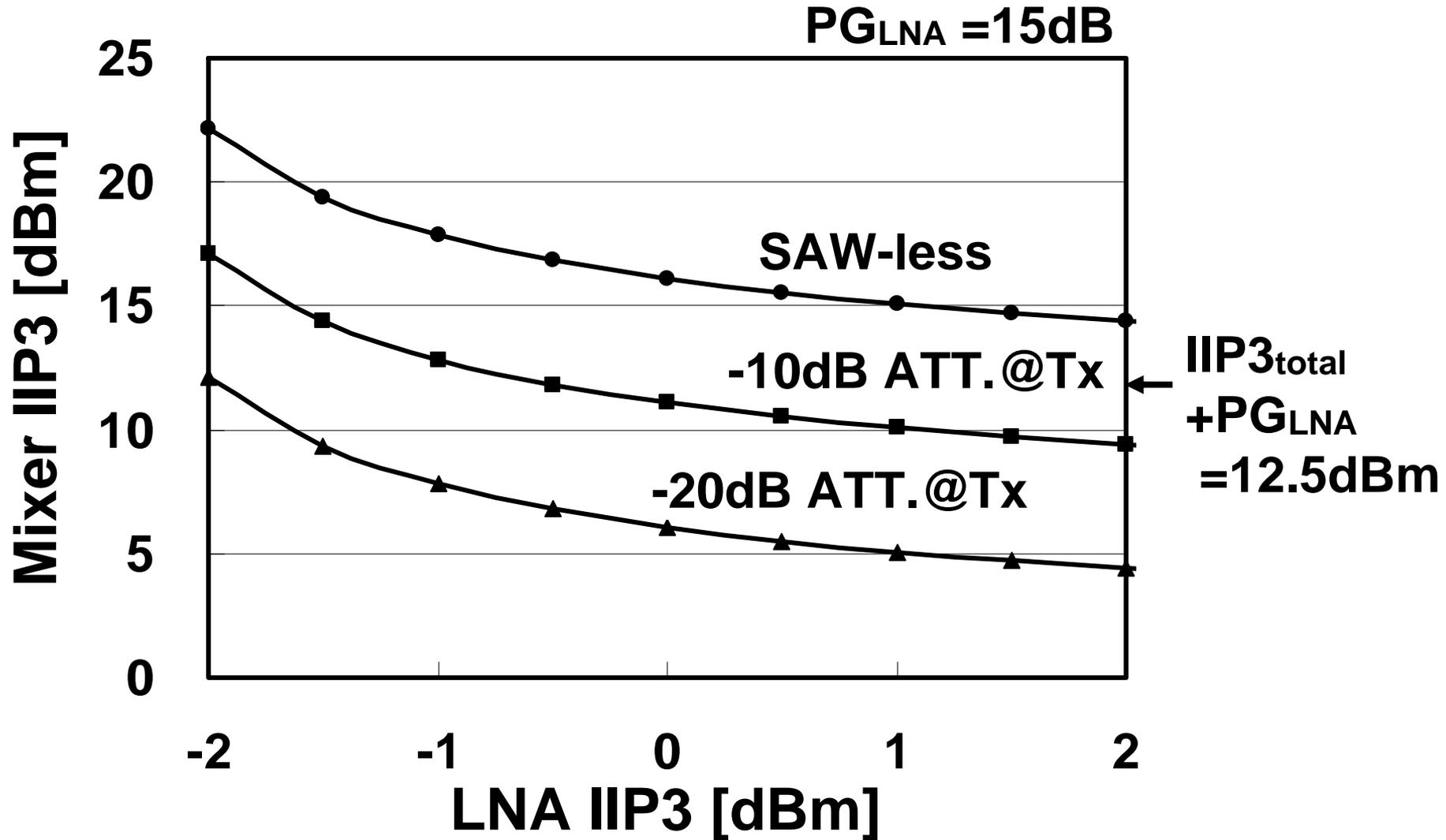
for out-of-band

for out-of-band

for both cases  
REFSENS=-110dBm  
PG=25dB  
IIP3=-2.5dBm  
IIP2=70dBm  
NF=2.5dB (3dB total)  
Dup.loss=3dB  
with  
P<sub>Tx</sub>=-30dBm  
P<sub>CW\_inter</sub>=-40dBm  
P<sub>CW\_out</sub>=-60dBm

from Panasonic

# Required IIP3 for SAW-less mixer



**IIP3 of -2.5dBm is required for the entire Rx chain.**

# Requirements for multi-standard Rx

Some kind of reconfiguration is required.

On-chip tunable filter is indispensable.

## Rx

- Band width **400MHz-6GHz**
  - GSM/UMTS/LTE, GPS, WLAN, BT, DTV/FM, etc
- Rx NF  $<2.5\text{dB}$  for Cellular, IIP3  $>-2.5\text{dBm}$  for UMTS
- Rx NF  $<2\text{dB}$  for GPS

## LNA

- **IIP3  $>0\text{dBm}$**
- **NF  $<2.2\text{dB}$**
- **PG = 15dB**

Mixer (with LNA of PG=15dB, NF=2.2dB, IIP3=0dBm)

- **NF  $<6\text{dB}$**
- **IIP3  $>16.1\text{dBm}$  without inter-stage filter**
- **IIP2  $>70\text{dBm}$  without inter-stage filter**

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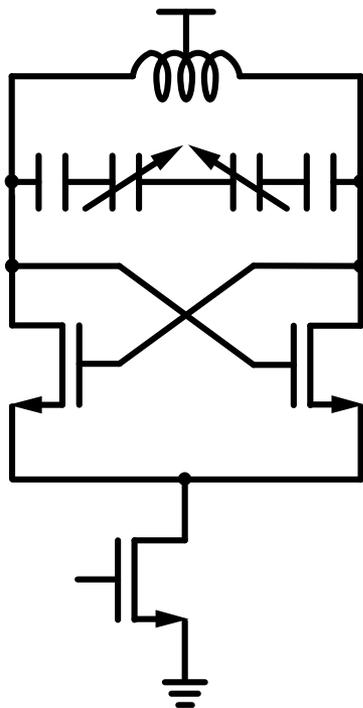
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# LO requirements

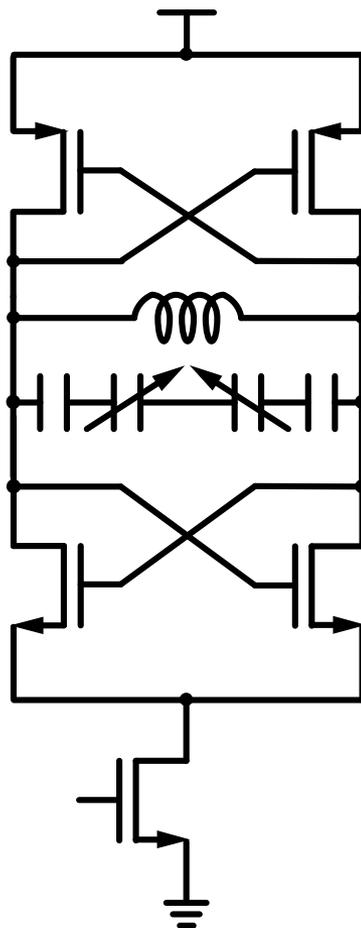
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- **10MHz-10GHz continuous tuning**
- **Low phase noise**
  - GSM850/900 -162dBc/Hz@20MHz-offset**
  - Q of on-chip inductor < 15**
  - Supply voltage <1.5V**
- **No spurs**
- **Quadrature outputs with less I/Q mismatch**
- **Low power consumption**
- **Small layout area**
  - smaller number of on-chip inductors**

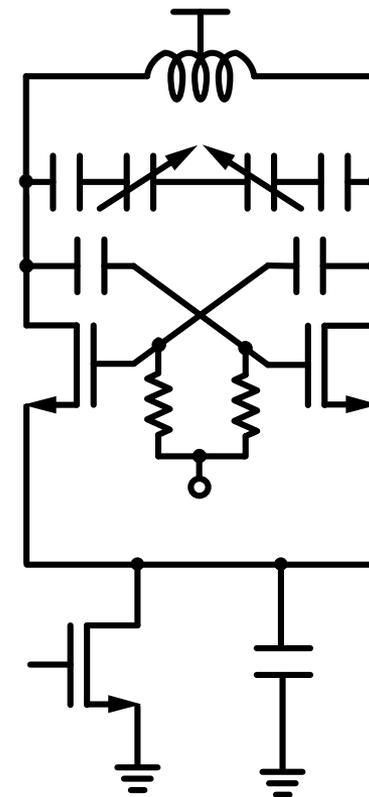
# VCO topologies



**(1) NMOS VCO**



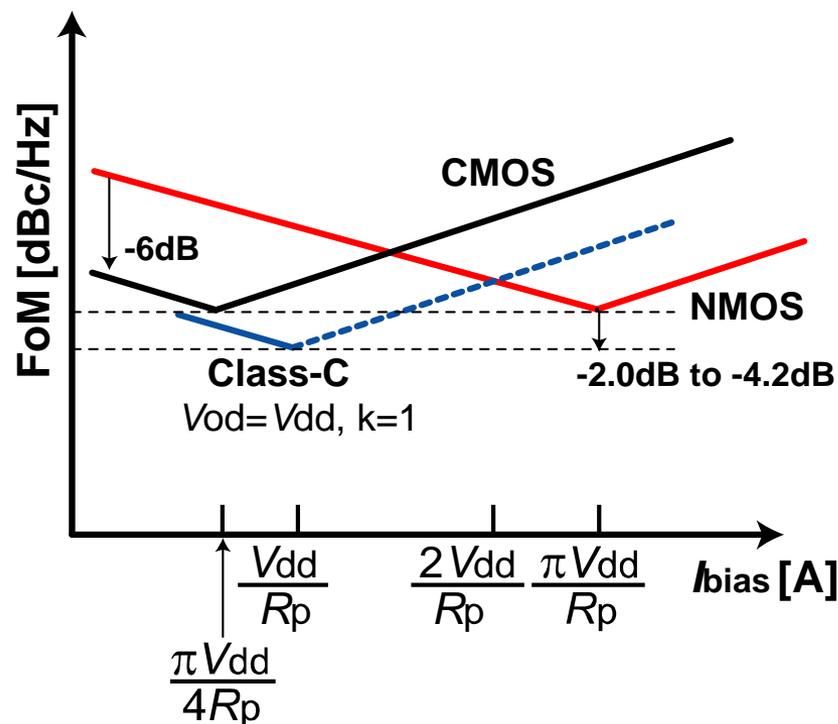
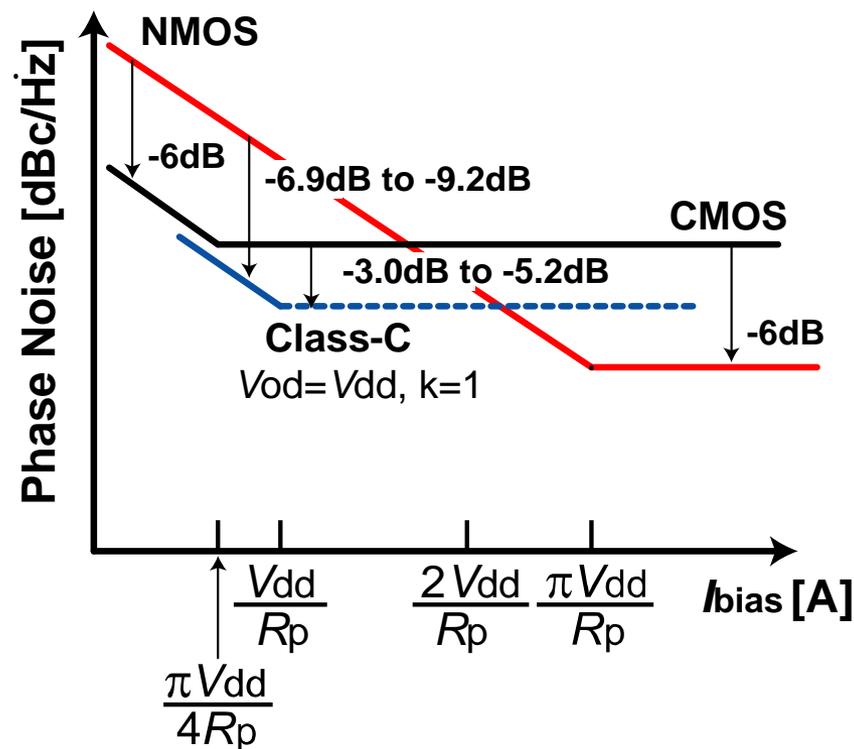
**(2) CMOS VCO**



**(3) Class-C VCO\***

\*A. Mazzanti and P. Andreani, JSSC 2008

# Theoretical limit of phase noise

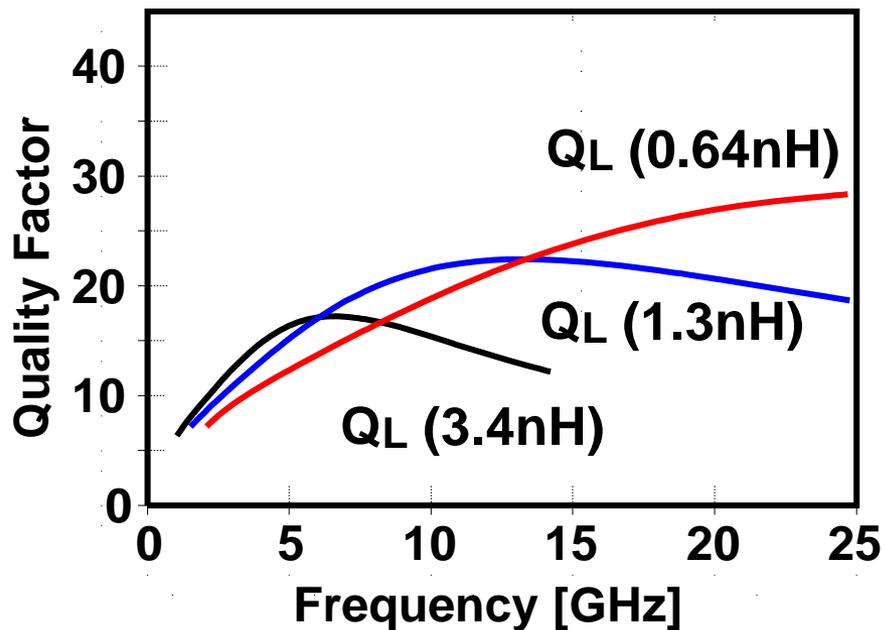


**NMOS VCO can realize the lowest phase noise theoretically.**

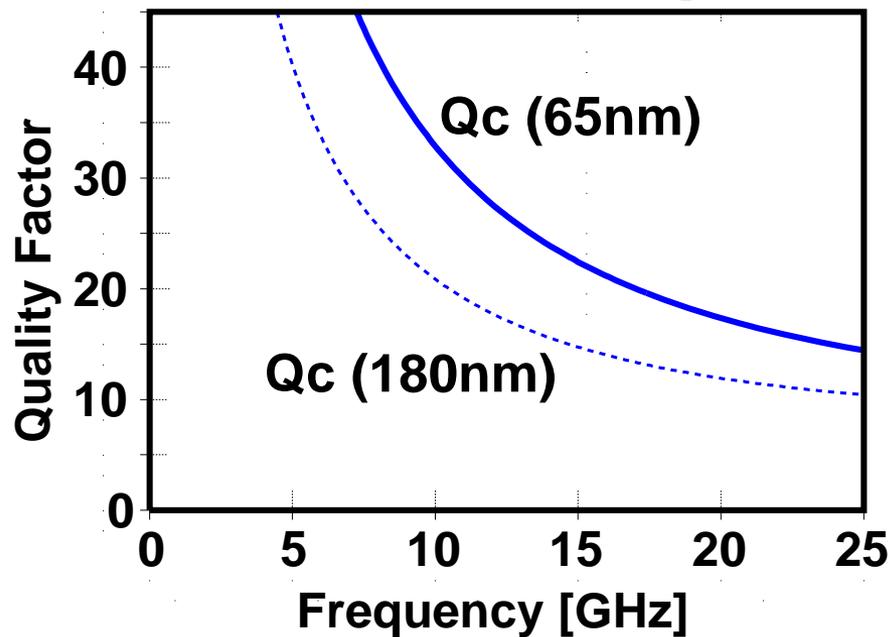
$$PN = 10 \log_{10} \left( \frac{\omega^3}{\Delta\omega^2} \frac{L}{Q} \frac{k_B T (1 + \gamma_n)}{4V_{DD}^2} \right)$$

# Limited Q-factor

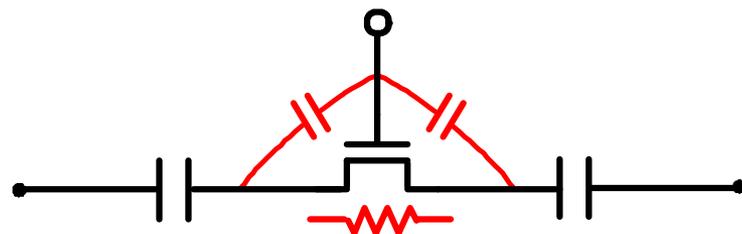
## Inductor



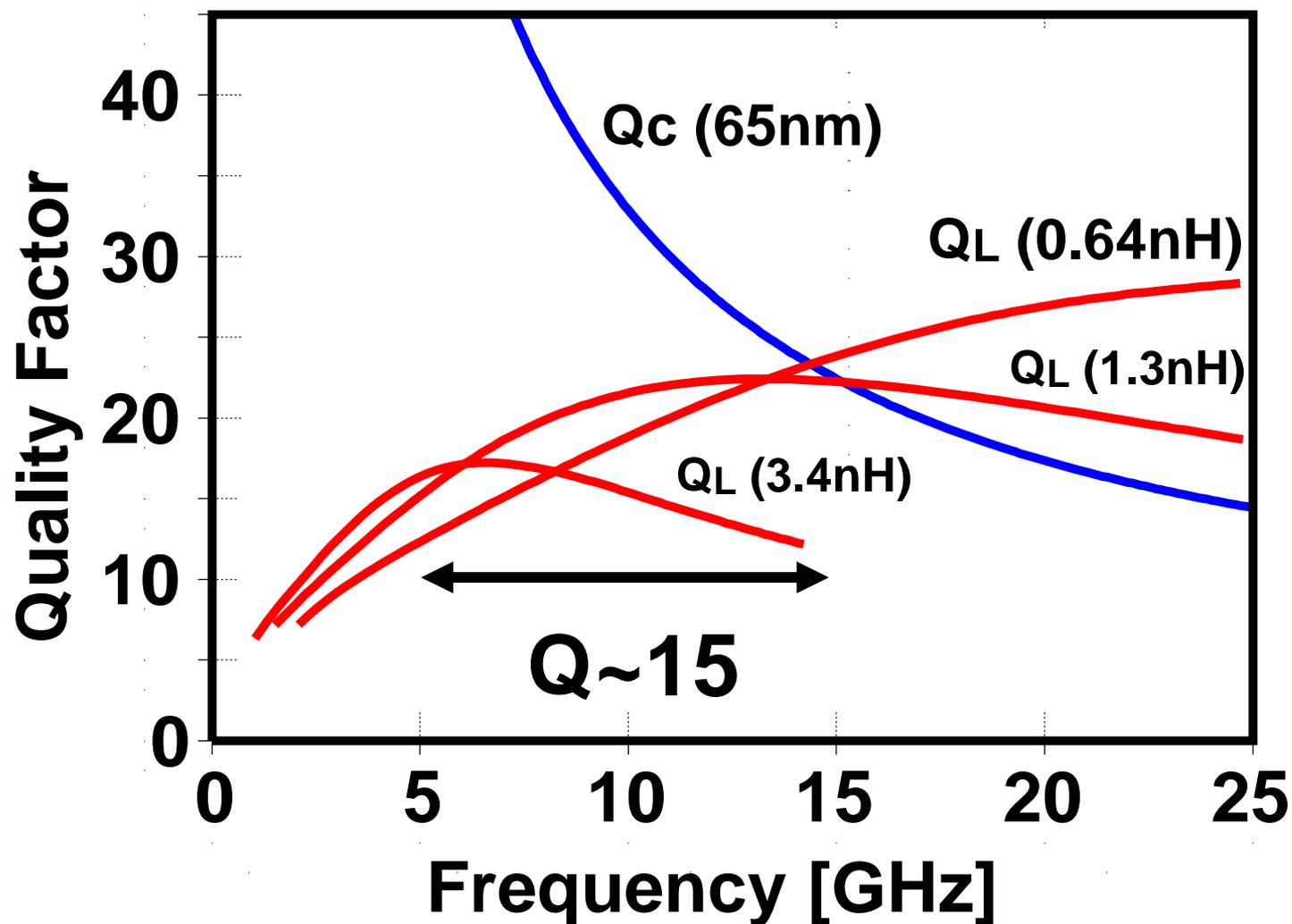
## Switched cap.



$$Q_L = \frac{\omega}{2} \left| \frac{1}{Z} \frac{\partial Z}{\partial \omega} \right|_{\omega=\omega_0}$$



# Q-factor of LC tank



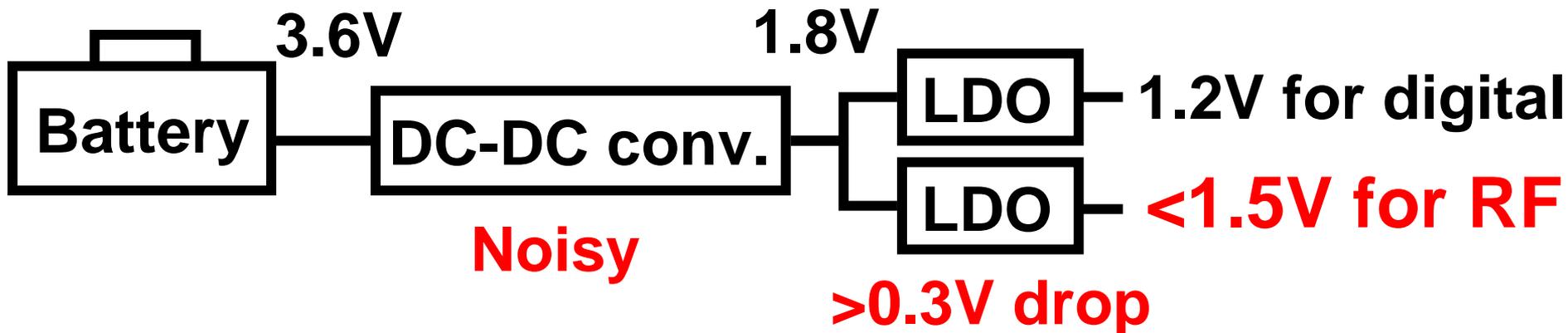
**5GHz-to-15GHz is better to obtain a high-Q LC resonator.**

# Supply voltage issues

- VCO Phase Noise
- LNA Linearity, PA Pout

$$PN = 10 \log_{10} \left( \frac{\omega^3}{\Delta\omega^2} \frac{L}{Q} \frac{k_B T (1 + \gamma_n)}{4V_{DD}^2} \right)$$

## Power supply for a mobile RFIC



# Required supply voltage for GSM

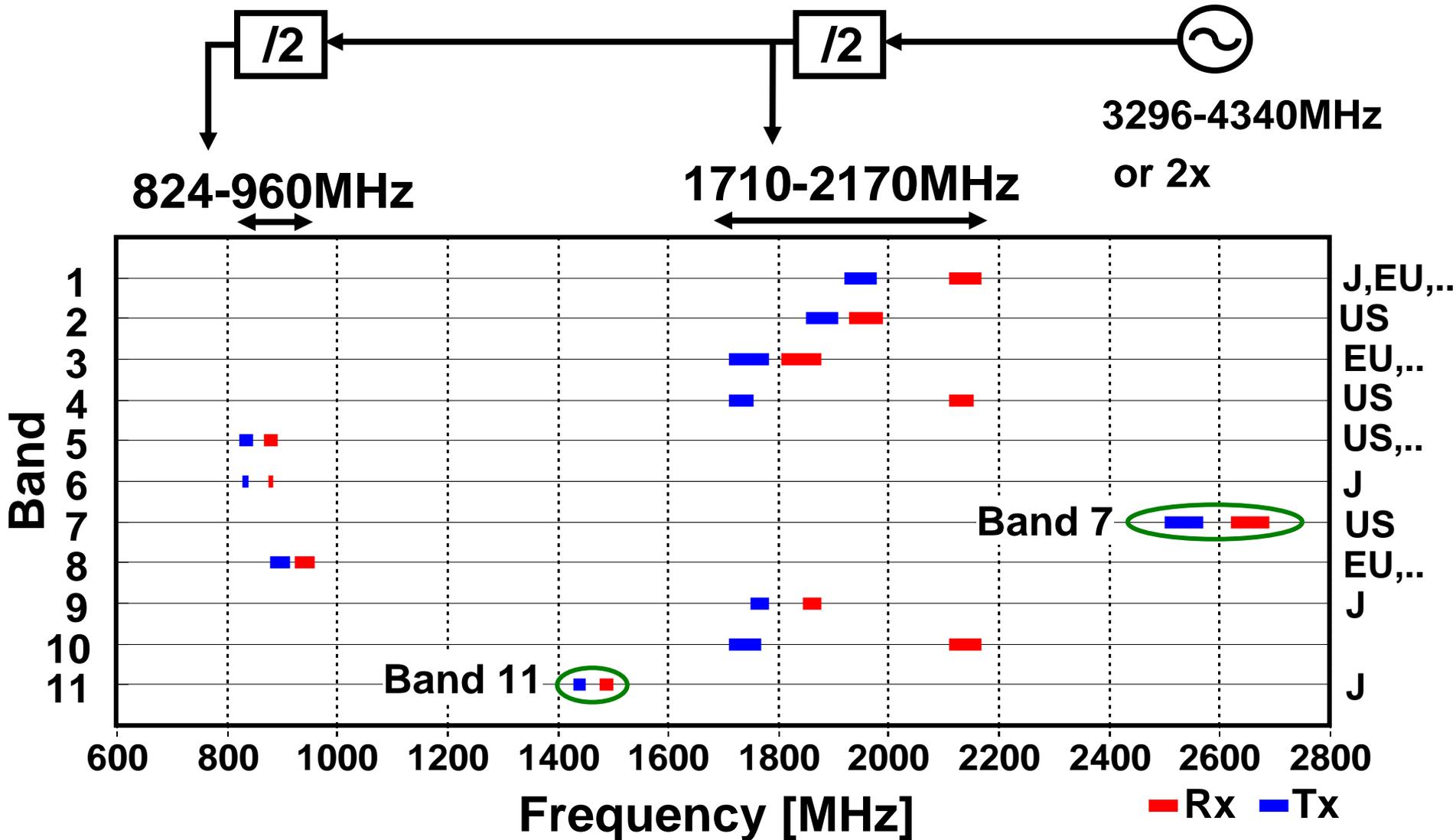
## GSM900 Tx LO: -165dBc/Hz@20MHz-offset

Q <sub>tank</sub>	V <sub>DD</sub> [V]	Ideal PN [dBc/Hz] +5dB @0.9GHz	Required I <sub>bias</sub> [mA]	P <sub>dc</sub> [mW]
Q=9 (L=3.4nH) @3.6GHz	1.2	-162	7.8	14.1+ $\alpha$
	1.5	-164	7.8	14.1+ $\alpha$
Q=12 (L=1.3nH) @7.2GHz	1.2	-164	5.8	10.5+ $\alpha$
	1.5	<u>-166</u>	5.8	10.5+ $\alpha$
Q=30 (ext.) (L=1.3nH) @7.2GHz	1.2	<u>-168</u>	1.5	2.7+ $\alpha$
	1.5	<u>-170</u>	1.5	2.7+ $\alpha$

**VCO cannot reach with low digital V<sub>DD</sub>.**

# LO generation for GSM/UMTS/LTE

conventional approach



# Requirements for multi-standard LO

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- **Satisfy all existing/possible wireless standards**
- **10MHz-6GHz continuous tuning with 1 inductor**
- **Fine tuning and fast settling for cognitive radios**
- **Low phase noise (GSM850/900)**
- **No spurs for wideband RF signal**
- **Quadrature outputs with less I/Q mismatch**
- **Low power consumption <10mW**

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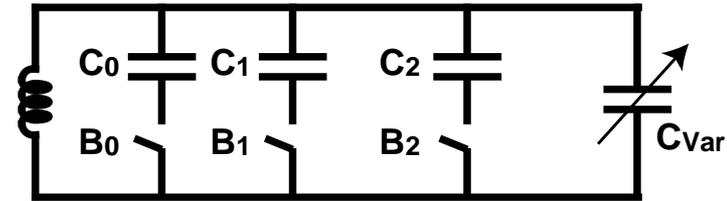
# Previous work for multi-band VCO

## ■ Switched-Capacitor Resonator

+ Reduced  $K_{vco}$

- QL is degraded at edge of tuning range

- Limited  $C_{max}/C_{min}$  (parasitic capacitance limited)



## ■ 1/2 Divider

+ Continuous wide tuning range

- Wide tuning range requirement for VCO

- Poor phase noise

Core-VCO:  $f_{max}/f_{min} = 2$



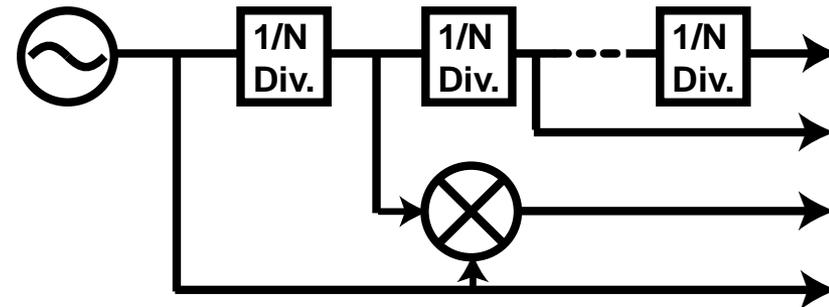
## ■ Dividers, Mixers

+ Small area

- Large power consumption

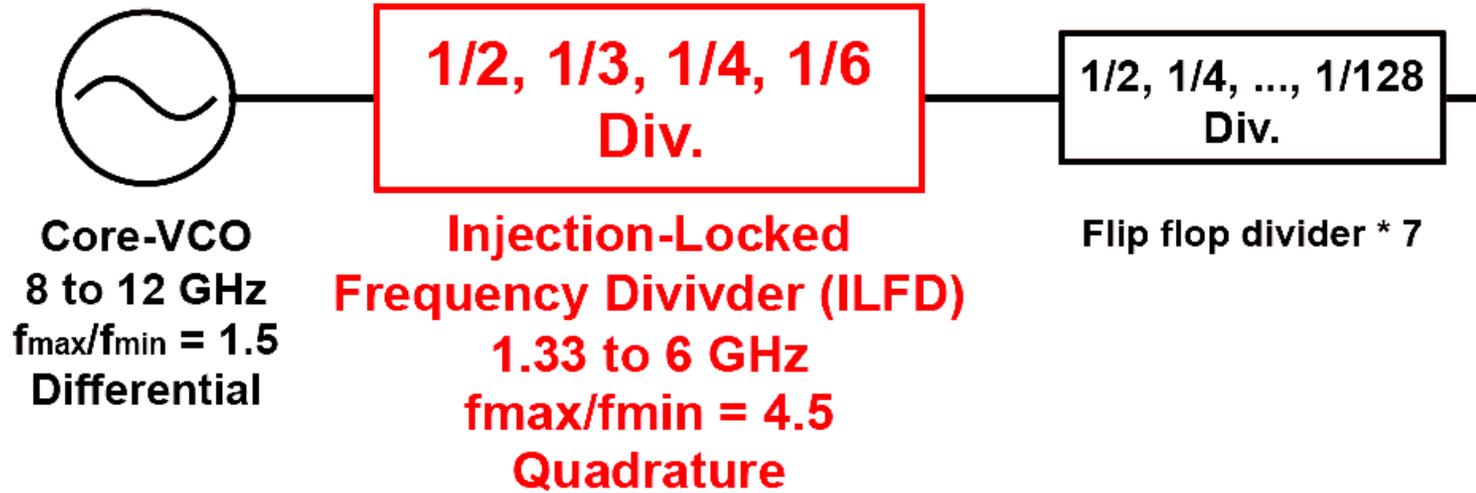
- Spurious tones

Core-VCO:  $f_{max}/f_{min} = 1.5$

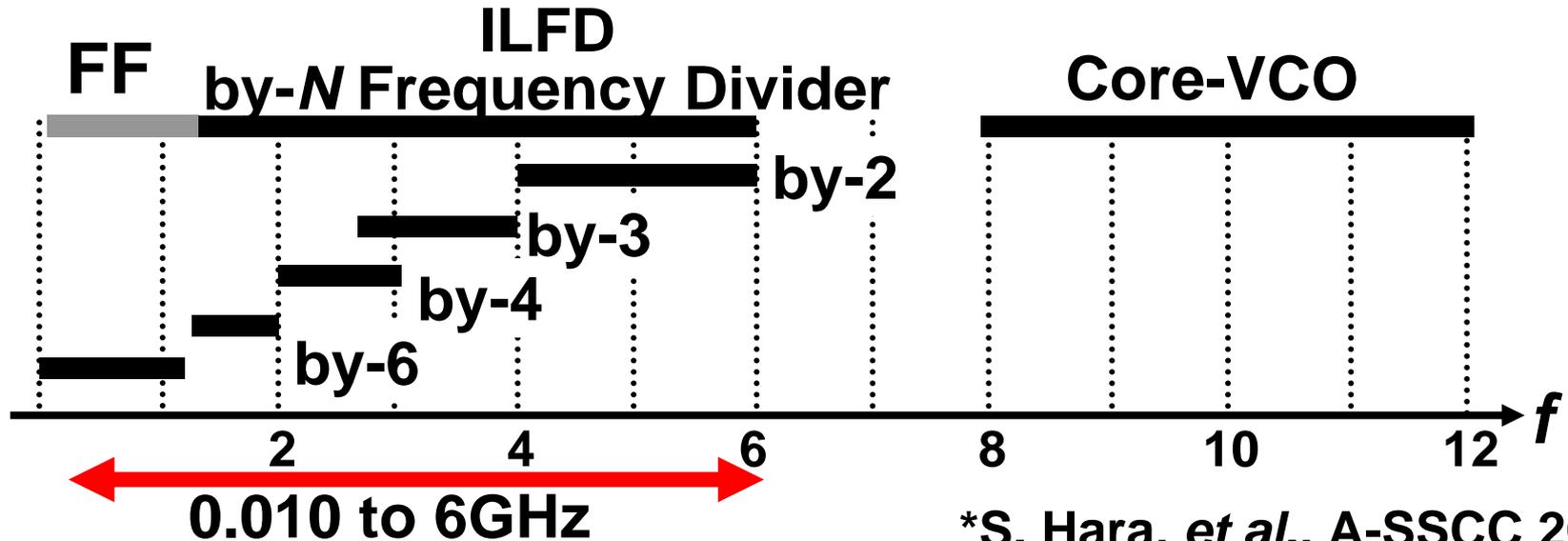


\*Z. Safarian, *et al.*, *CICC*, Sep. 2008.

# Proposed wideband VCO

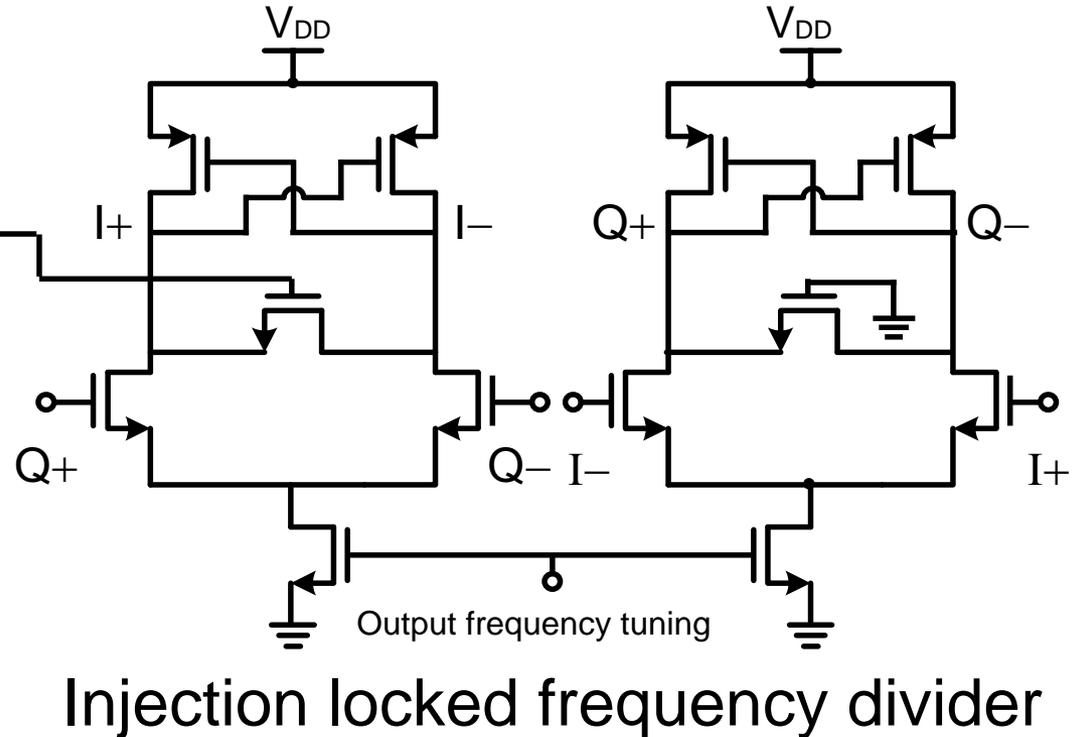
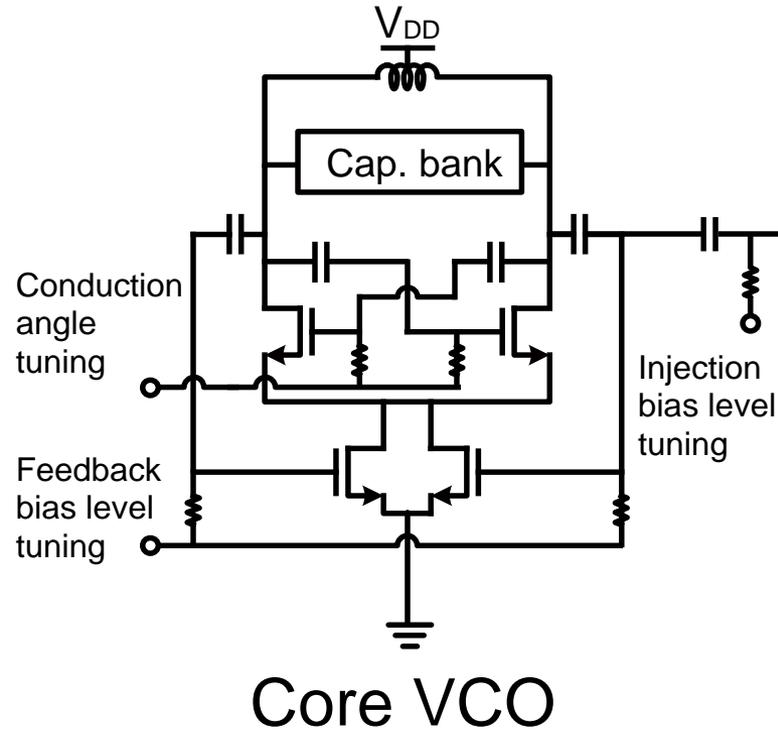


Narrow required tuning range, No spur, Quadrature output



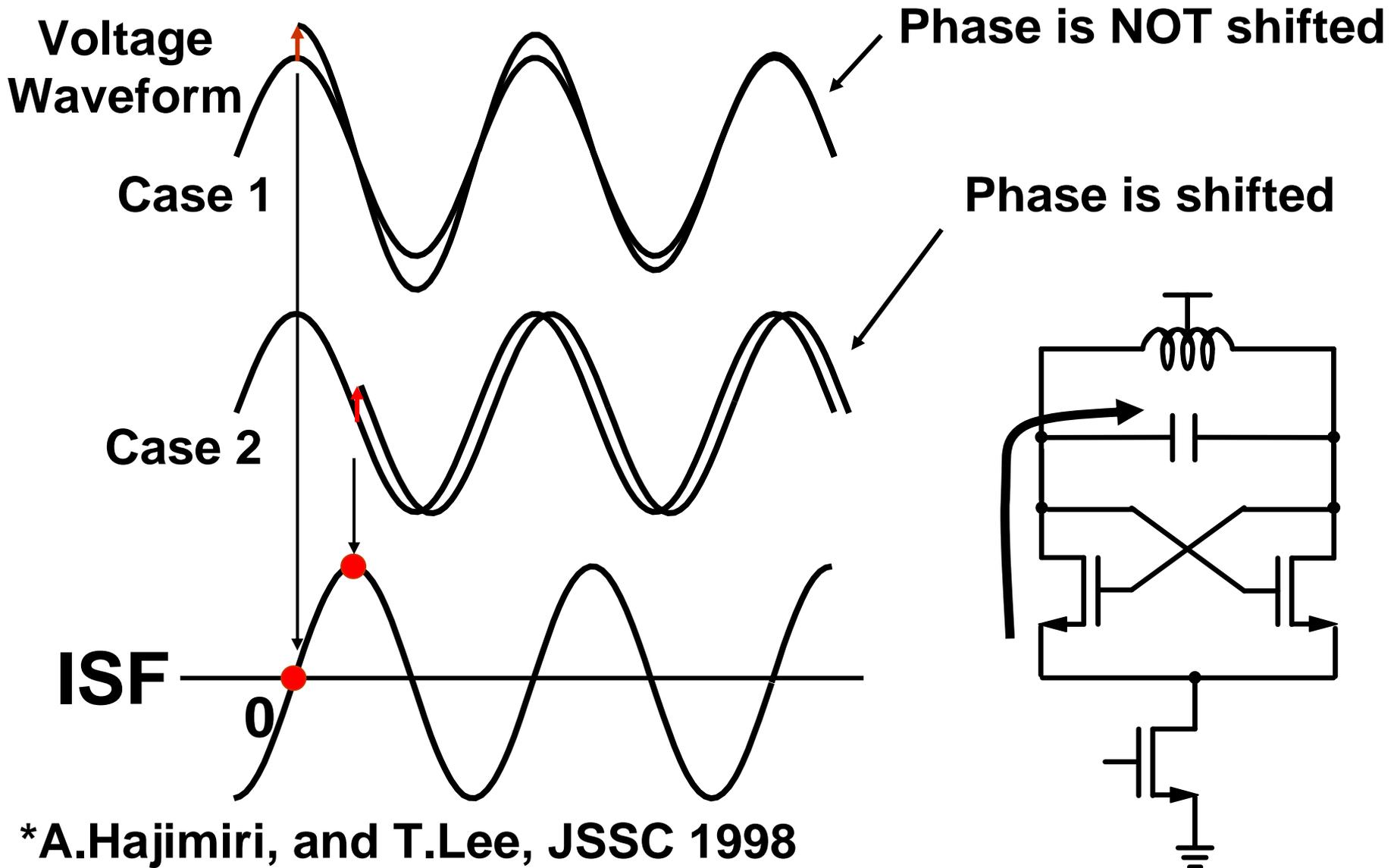
\*S. Hara, et al., A-SSCC 2009

# Circuit schematics



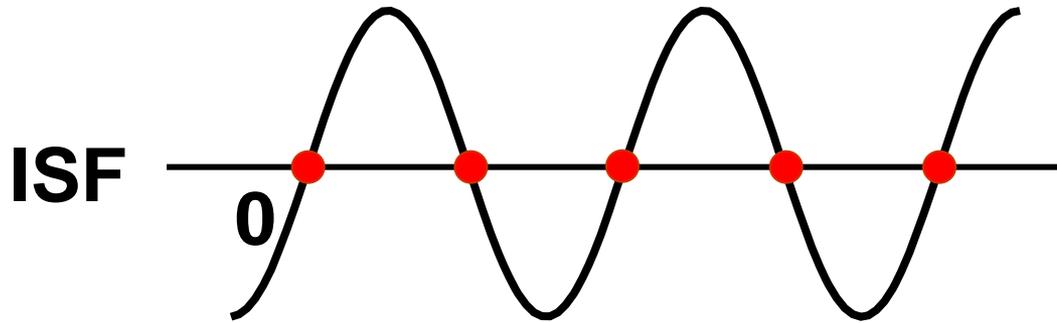
- **ILFD generates 1.33 to 6.0 GHz output.**
- **Lower frequency (under 1.33GHz ) can be obtained by using FF dividers.**

# Impulse Sensitivity Function (ISF\*)

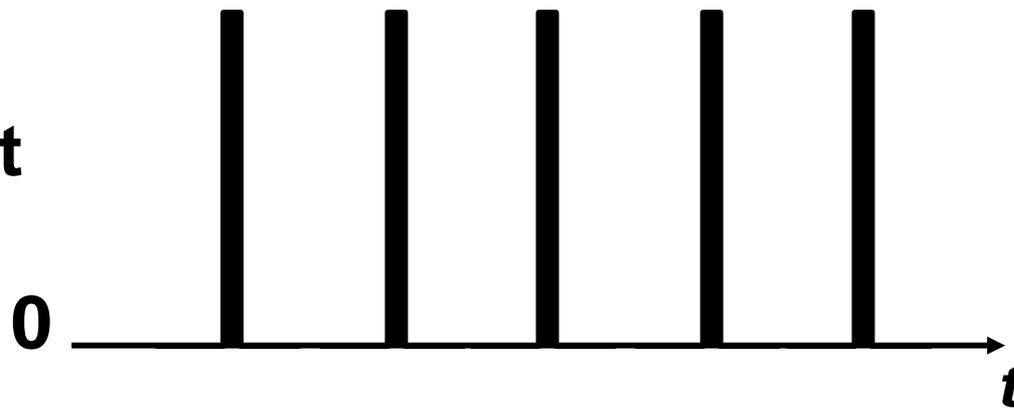


\*A.Hajimiri, and T.Lee, JSSC 1998

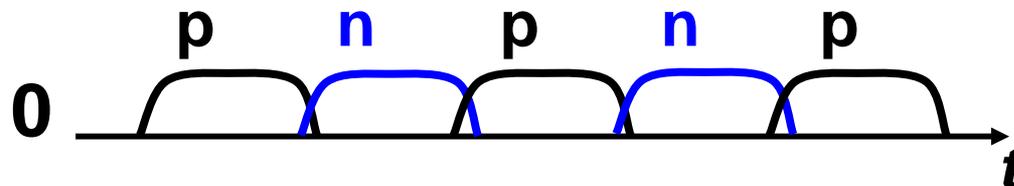
# Ideal Current Conduction



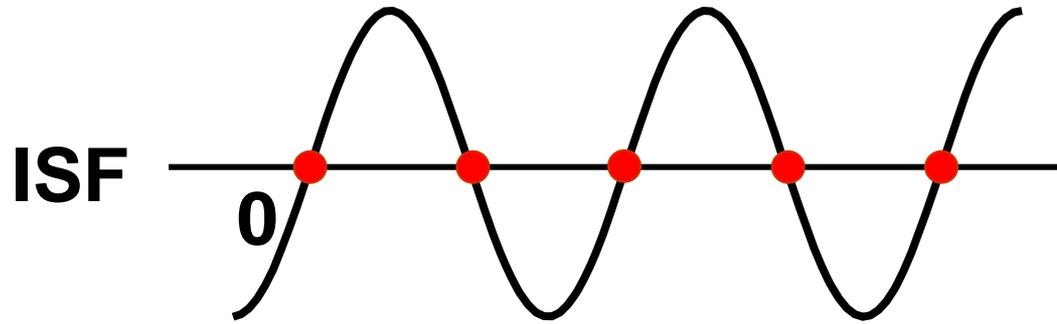
Ideal Current



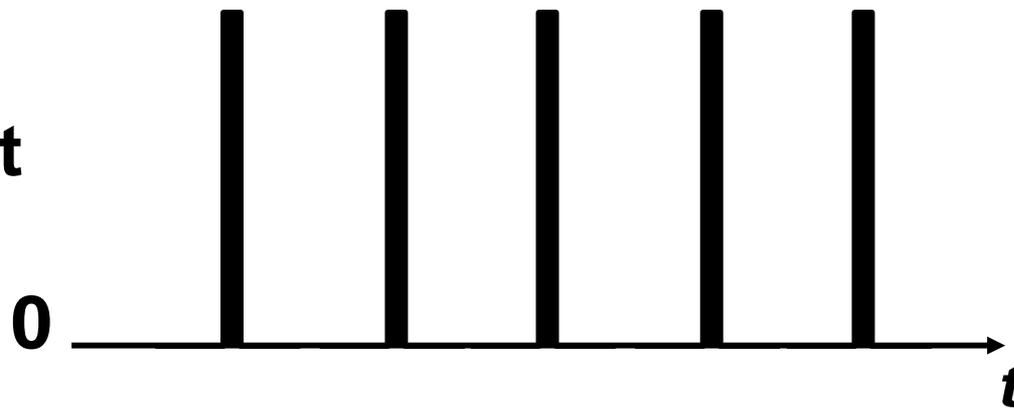
Conventional  
LC-VCO



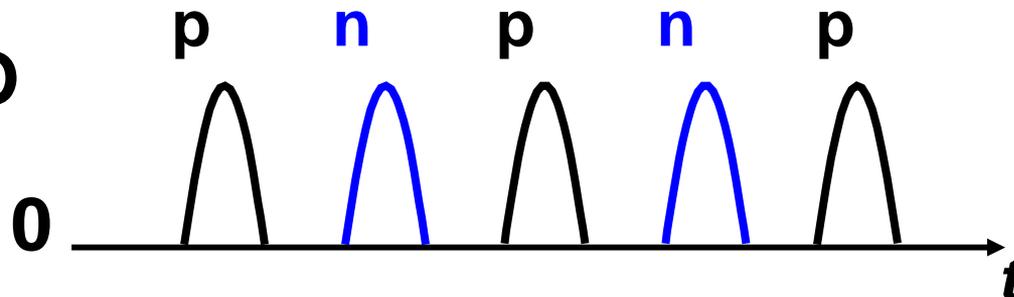
# Current conduction of class-C VCOs



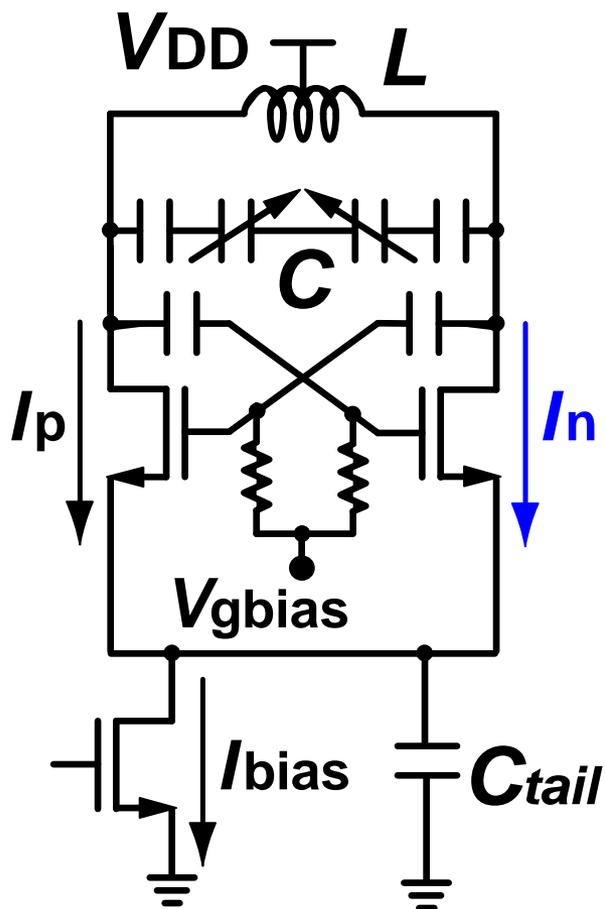
Ideal Current



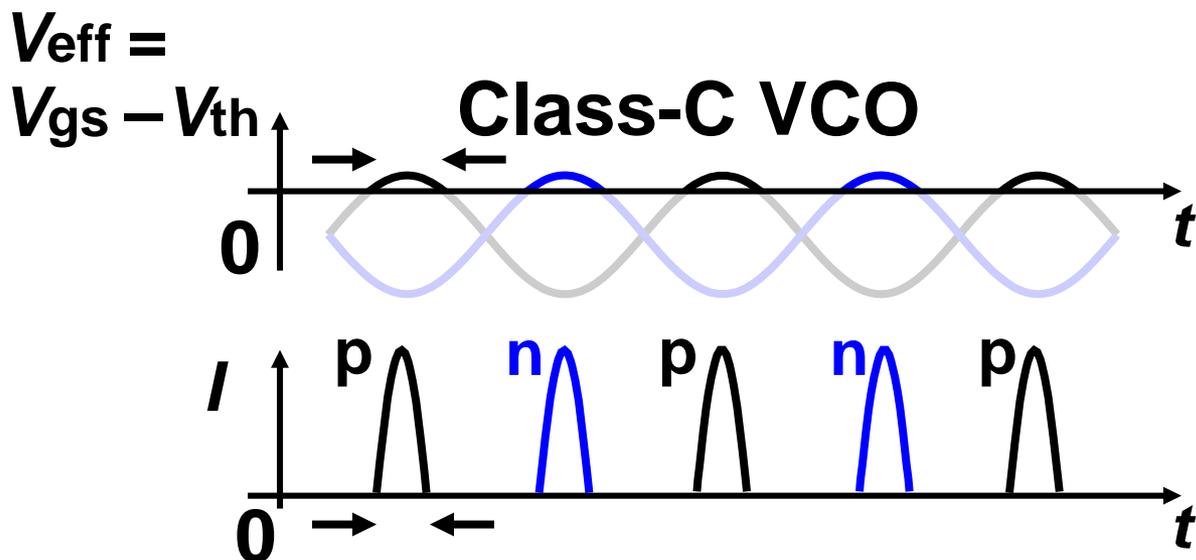
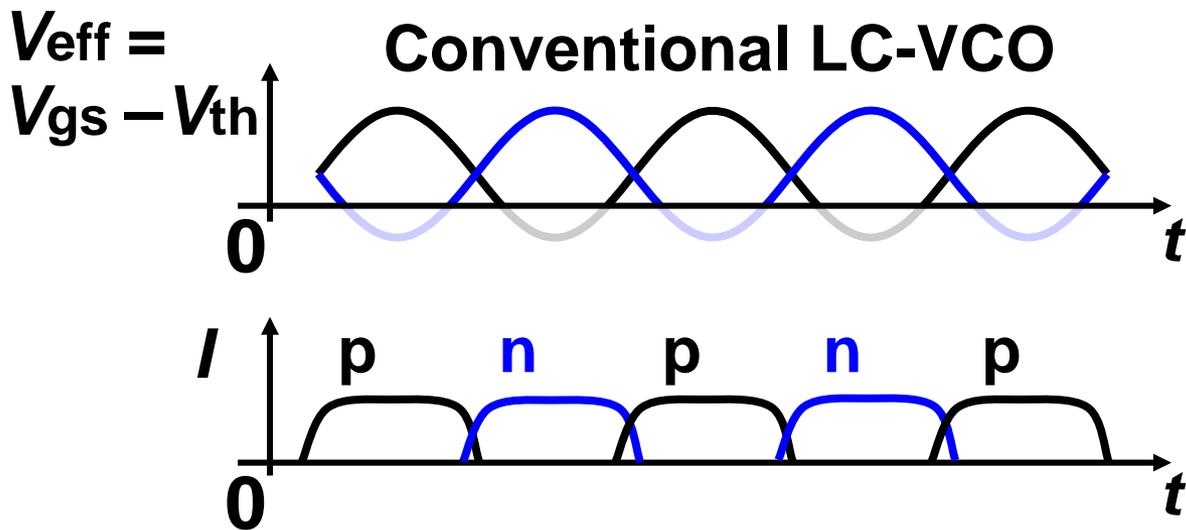
Class-C VCO



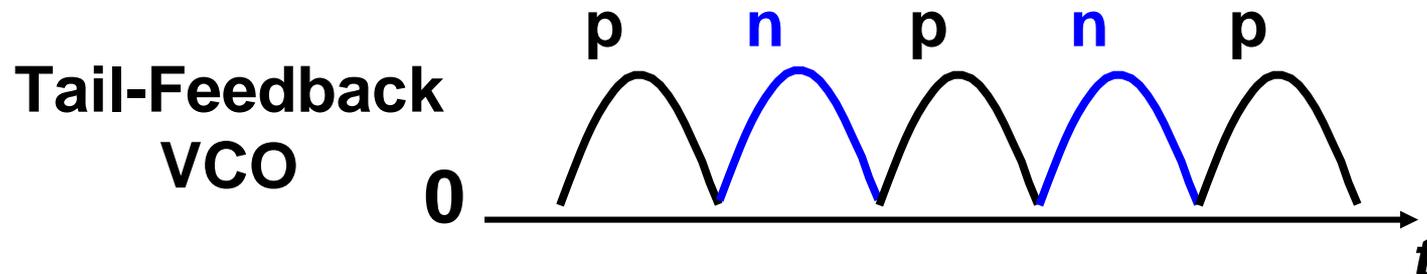
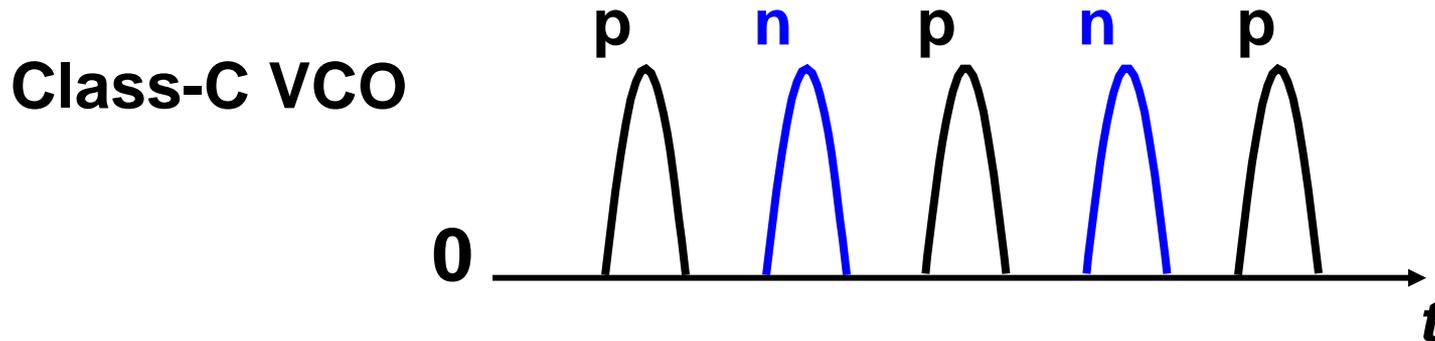
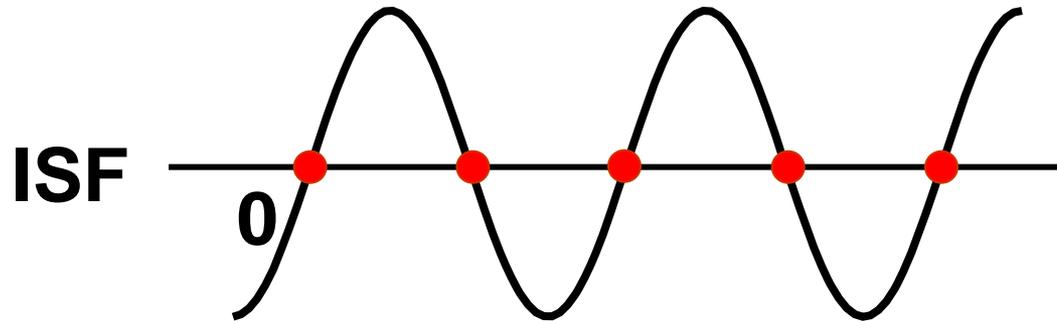
# Class-C VCO



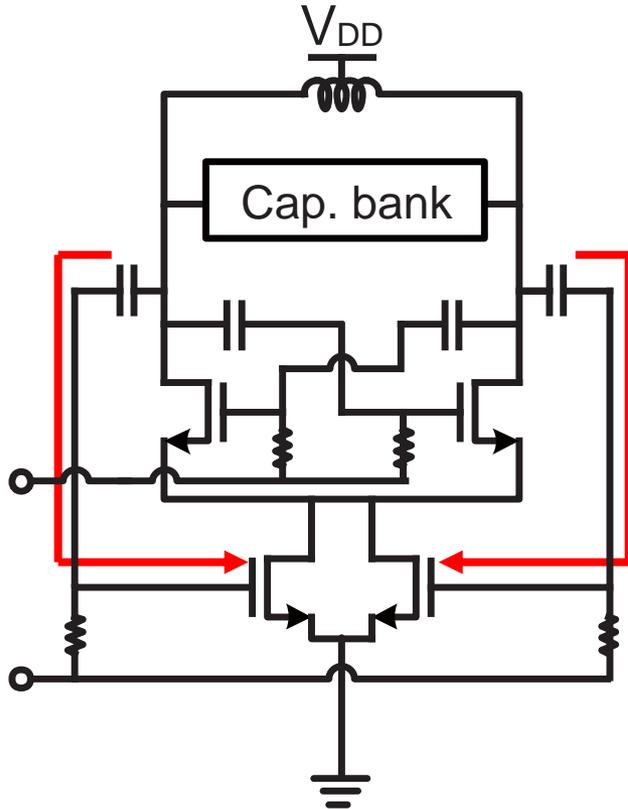
\*A. Mazzanti, *et al.*,  
JSSC 2008



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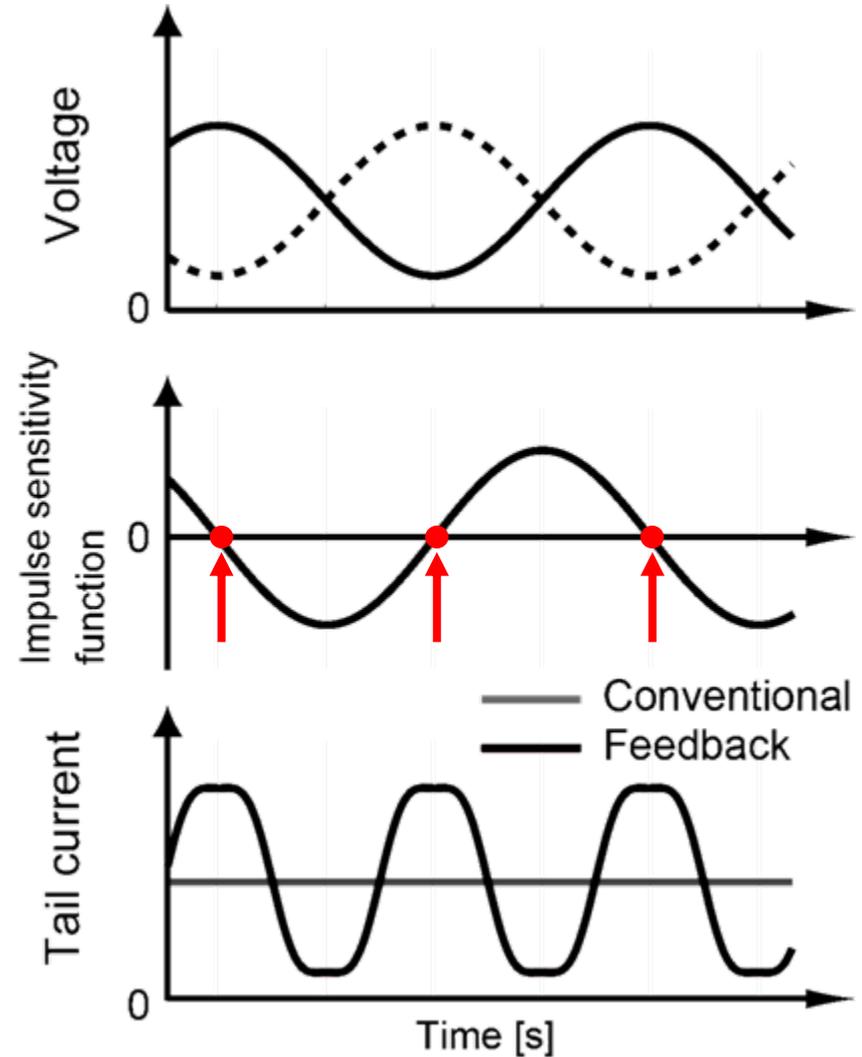


# Tail-feedback VCO

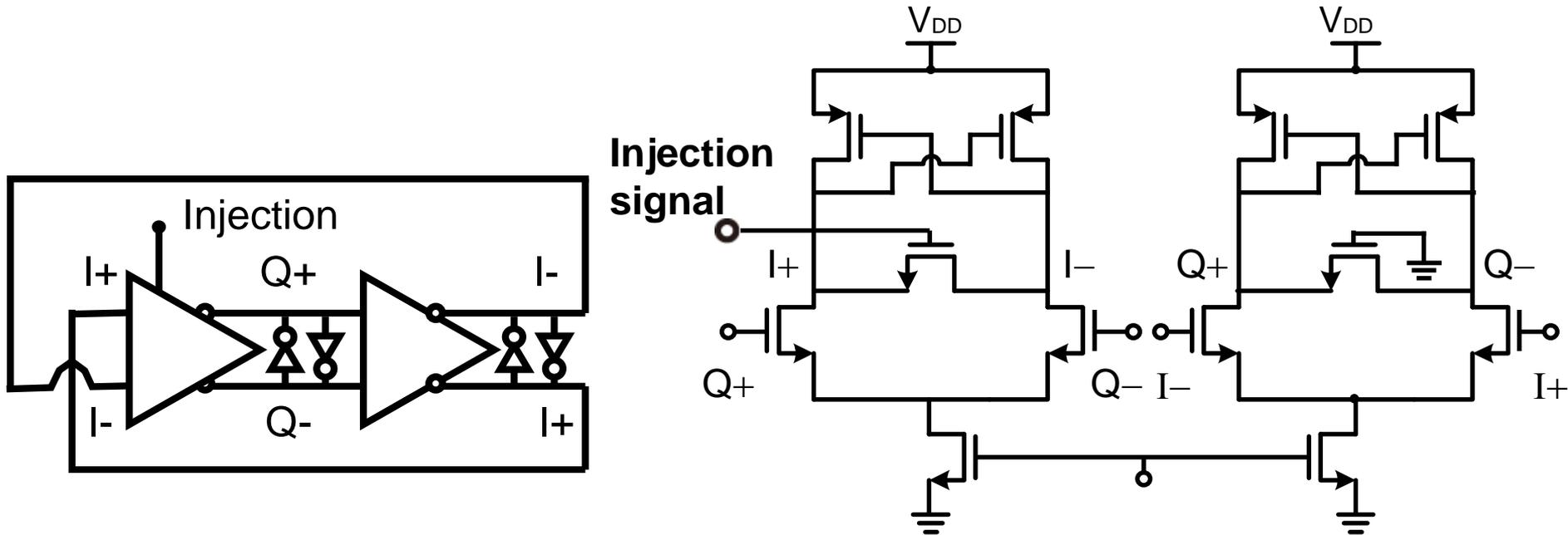


**Tail feedback**  
**3.5dB phase noise improvement**

- **Tuning range : 8.0 to 12.0 GHz**



# Injection Locked Frequency Divider

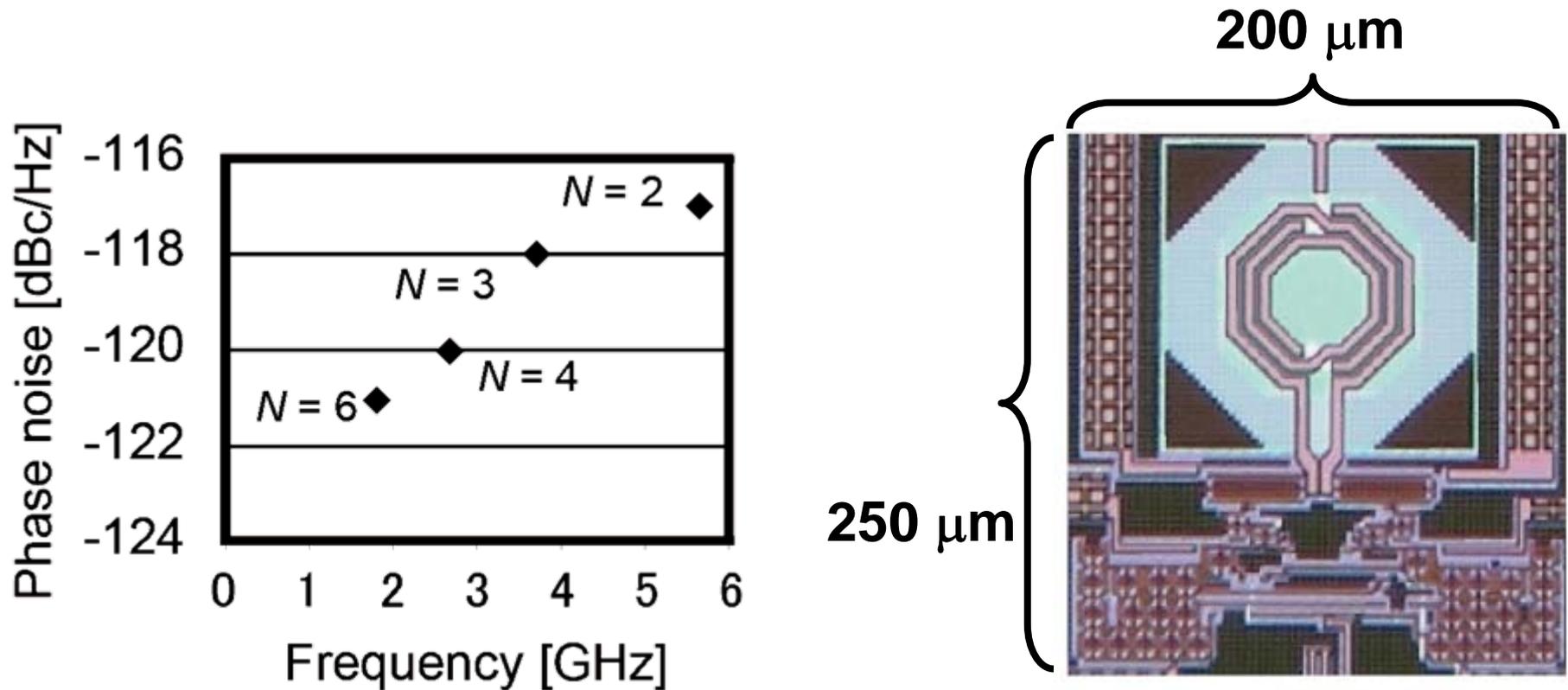


**2-stage differential ILFD is utilized.**

**Tuning range : 1.3 to 6.0 GHz**

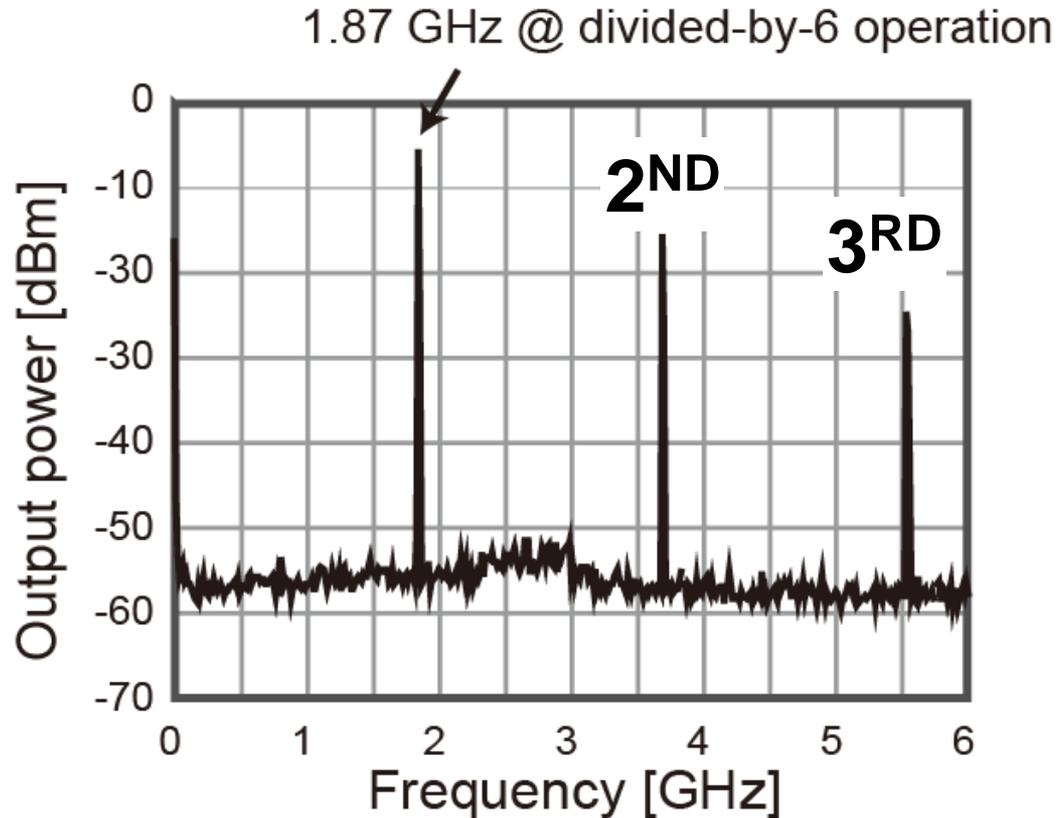
**Merit: Quadrature output, No Spur,  
Wide frequency range**

# Measurement Result



**Fabricated by 90 nm CMOS Process**

# Output spectrum



**Even harmonics can be canceled by differential config.**  
**Odd harmonics can be canceled by harmonic-rejection mixer.**

# VCO performance

<b>Technology</b>	<b>Standard 90nm CMOS</b>
<b>Supply voltage</b>	<b>1.2 V</b>
<b>Power consumption of VCO core</b>	<b>4.8 - 10.2 mW</b>
<b>Power consumption of ILFD</b>	<b>1.0 - 1.3 mW</b>
<b>Power consumption of FF dividers</b>	<b>- 0.1 mW</b>
<b>Total power consumption</b>	<b>5.9 - 11.2 mW</b>
<b>Tuning range</b>	<b>9.3 MHz - 5.7 GHz</b>
<b>Chip area</b>	<b>250 <math>\mu\text{m}</math> x 200 <math>\mu\text{m}</math></b>

# VCO measurement summary

	This work*	VLSI 2009**	RFIC 2009***
Architecture	VCO with ILFD	QVCO with mixer and dividers	2VCOs and dividers
Divide ratio	2,3,4,6...	2,3,4,5,6,8,10	2,4,8,16,32...
Tuning range of core LC-VCO	$\pm 20$ %	$\pm 20$ %	$\pm 33.3$ % (total)
Output freq.	0.009 - 5.7 GHz	1 - 10 GHz	0.1 - 5.0 GHz
Power cons.	<b>5.9 - 11.2 mW</b>	31 mW	19.8 mW
FoMT	<b>-210 dBc/Hz</b>	-194 dBc/Hz	-209 dBc/Hz
Area	<b>0.05 mm<sup>2</sup></b>	0.29 mm <sup>2</sup>	0.22 mm <sup>2</sup>

\*S. Hara, *et al.*, A-SSCC, Nov. 2009

\*\*B. Razavi, *VLSI Circuits*, June 2009.

\*\*\*P. Nuzzo, *et al.*, RFIC, June 2009.

# Summary and Conclusion

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- A differential LC-VCO and injection locked frequency divider are utilized instead of a QVCO and SSBMs to reduce spurious, layout area, and power consumption.
- The proposed wideband VCO can achieve wide tuning range with the best  $FoM_T$ .

**FTR=199% (9.3MH-5.7GHz)**

**FoM<sub>T</sub>=-210dBc/Hz**

# Outline

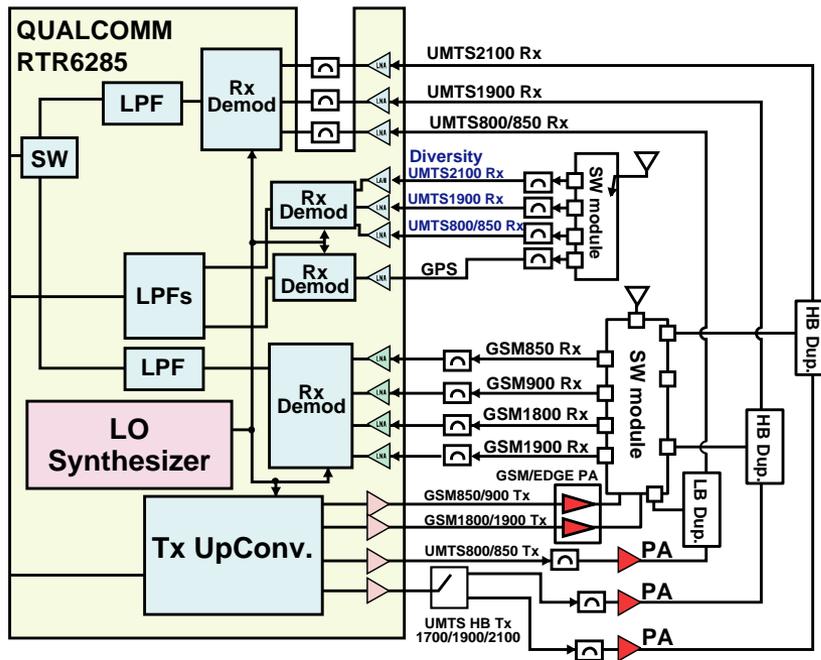
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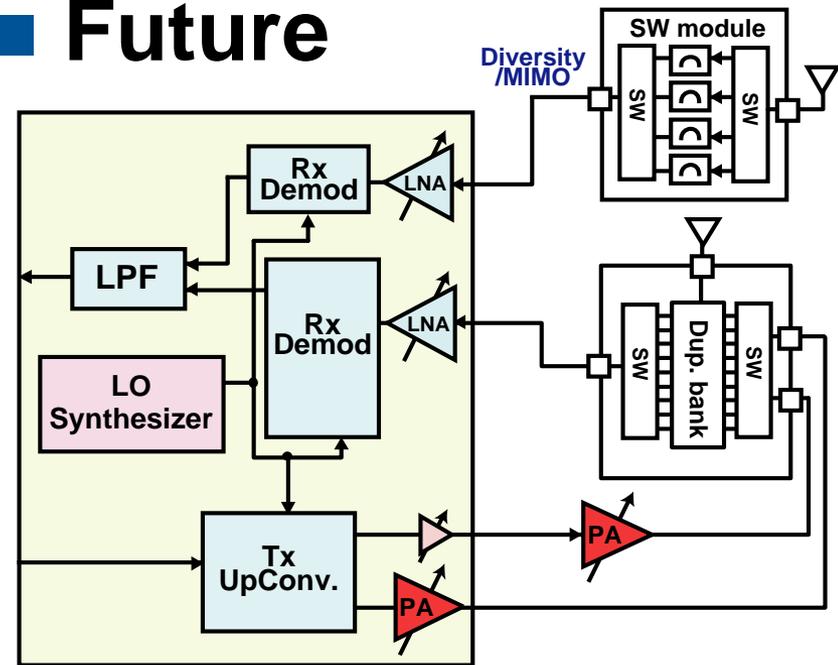
# Tx requirements

- On/off-chip tunable/switchable multi-standard PA
- Must keep the same Pout/PAE with smaller total footprint size and less number of components

## ■ Present



## ■ Future



**tunable/switchable**

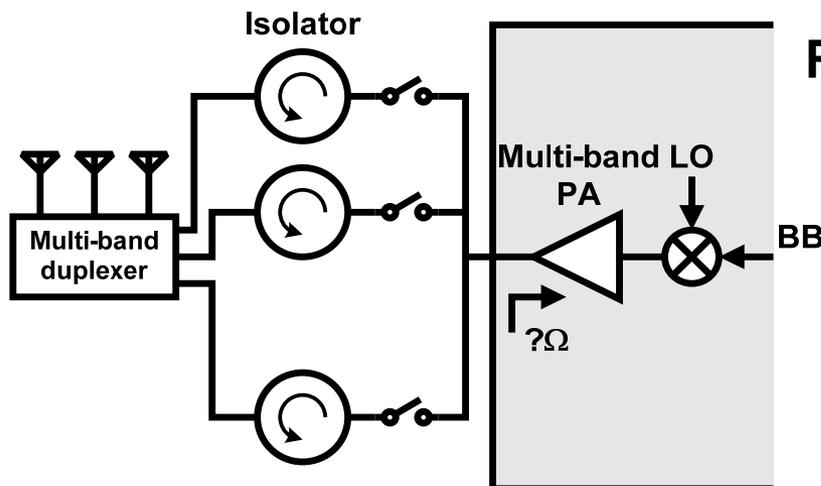
# Challenge of tunable CMOS PA

- Tunable CMOS PA with tunable impedance matching to reduce external components

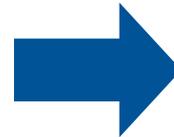
- isolators

- Reduce reflection due to impedance mismatch
- Protect PAs from reflected wave

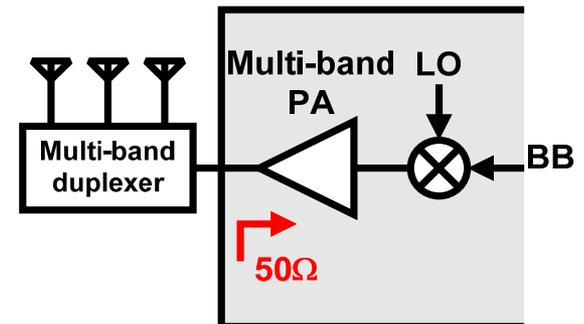
## ■ Conventional



Reducing off-chip components



## ■ Proposed



# Output impedance tuning 1

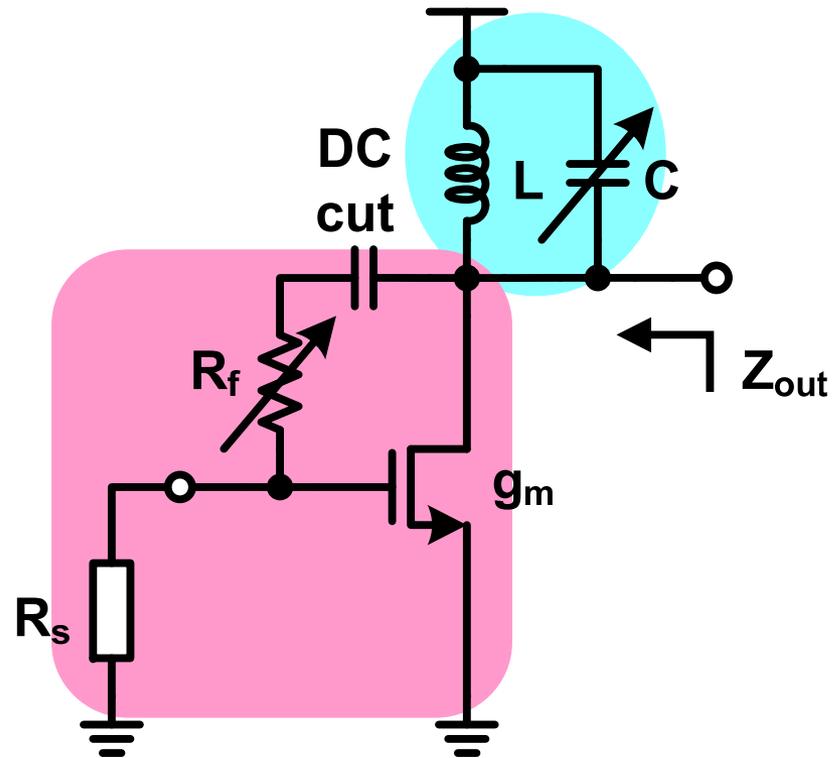
If  $r_{ds} = \infty$ ,

$$Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{1}{j\omega C} \parallel (R_L + j\omega L)$$

When  $f = \frac{1}{2\pi\sqrt{LC}}$

(Resonance frequency)

$$Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{L}{CR_L}$$



$R_s$  : source impedance ( $50\ \Omega$ )

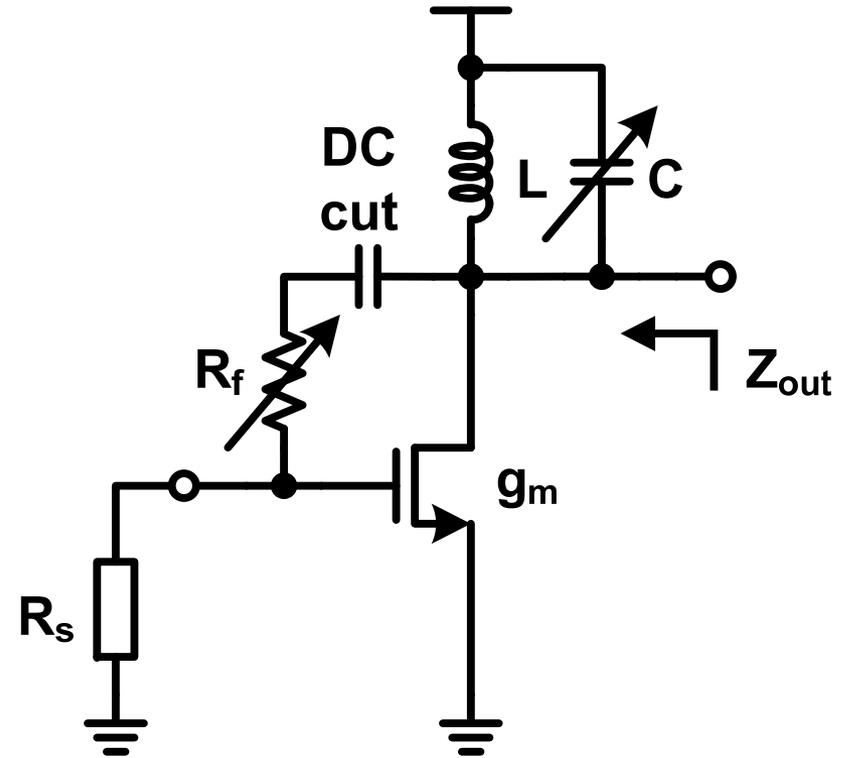
$R_L$  : inductor parasitic resistance

**Tune C to cancel imaginary part of  $Z_{out}$  at arbitrary frequency**

# Output impedance tuning 2

$$Z_{out} = \frac{R_f + R_s}{g_m R_s + 1} \parallel \frac{L}{CR_L}$$

- Tune  $R_f$  to match  $Z_{out}$  to  $50 \Omega$
- $Z_{out}$  depends on the value of  $C$ , so  $R_f$  needs to be adjusted according to the matching frequency

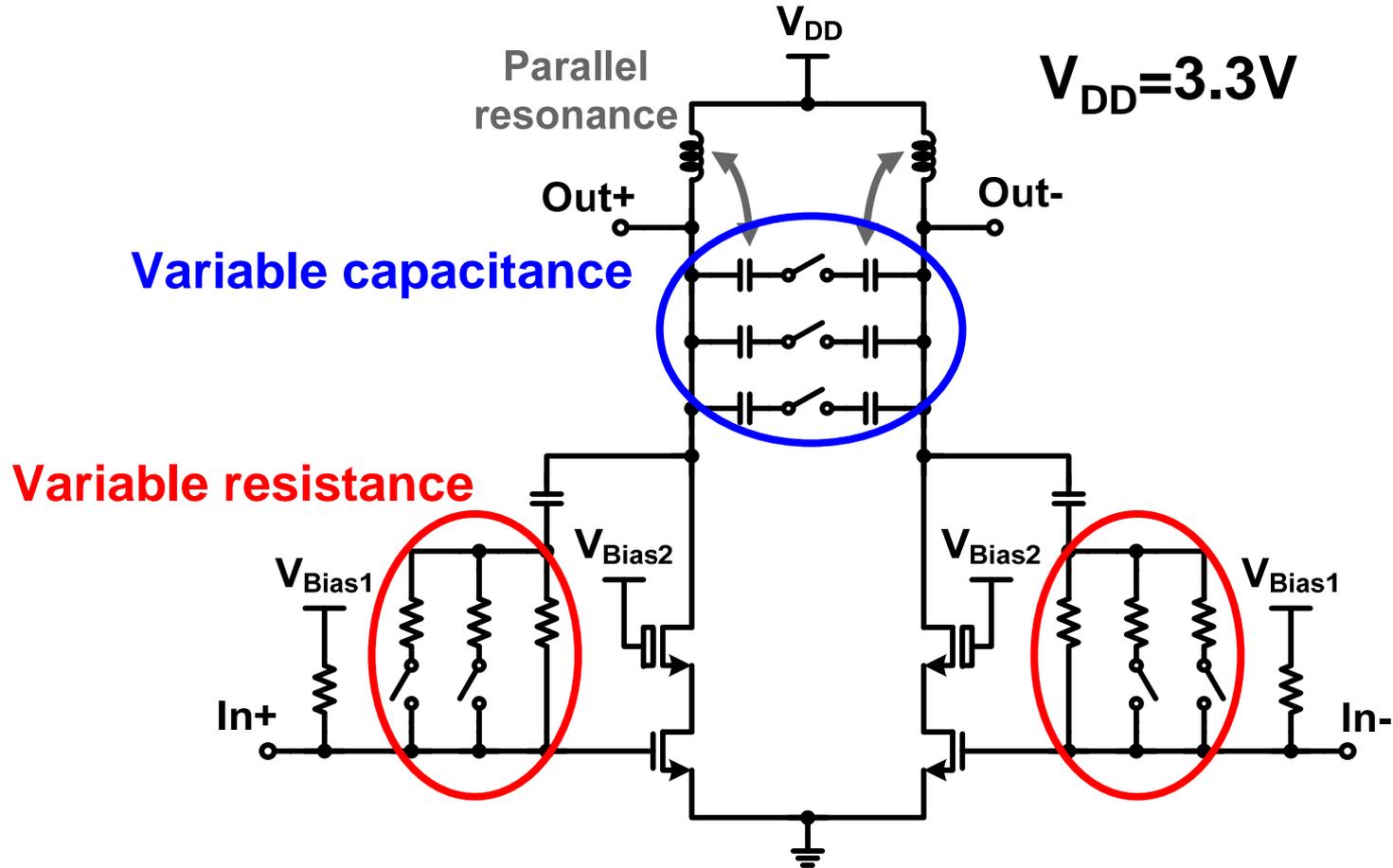


$R_s$  : source impedance ( $50 \Omega$ )

$R_L$  : inductor parasitic resistance

**Cascoded thick-oxide transistors are utilized because of larger  $r_{ds}$  and voltage-stress robustness.**

# Schematic of the proposed PA

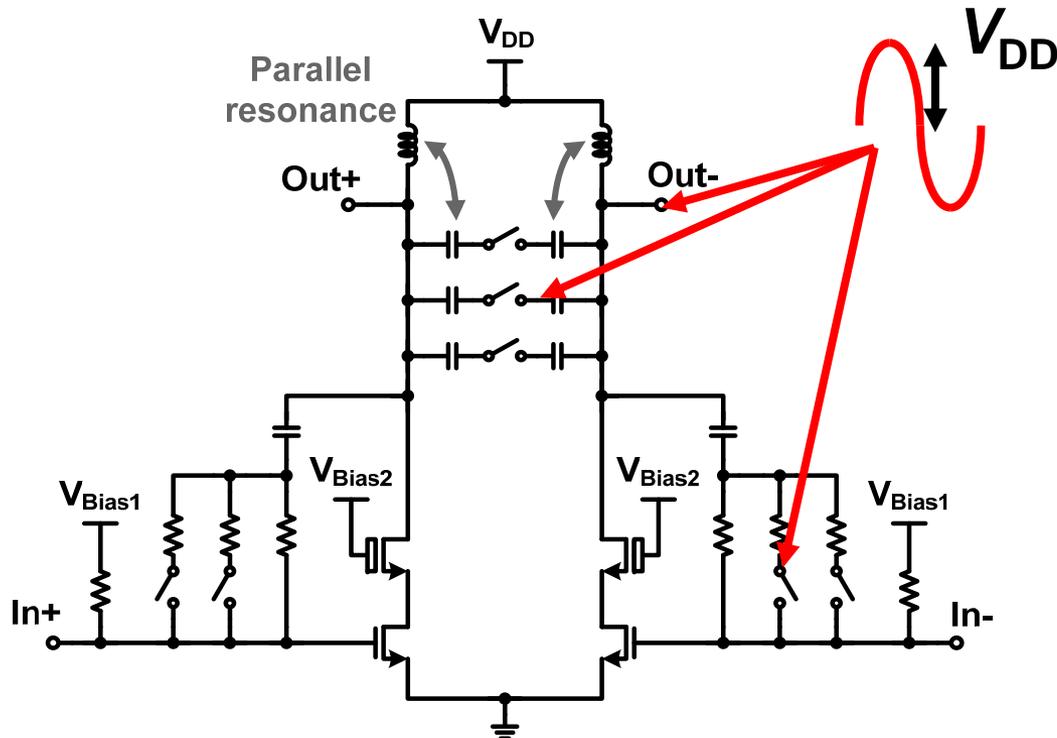


- Change output matching band by switching C and R
- Differential topology for 3dB larger  $P_{sat}$

# Voltage stress of switches

- Maximum voltage swing at output node is about  $V_{DD}=3.3V$
- The same voltage is applied to switches when they are off

➔ Thick oxide nMOS is applied as a switch

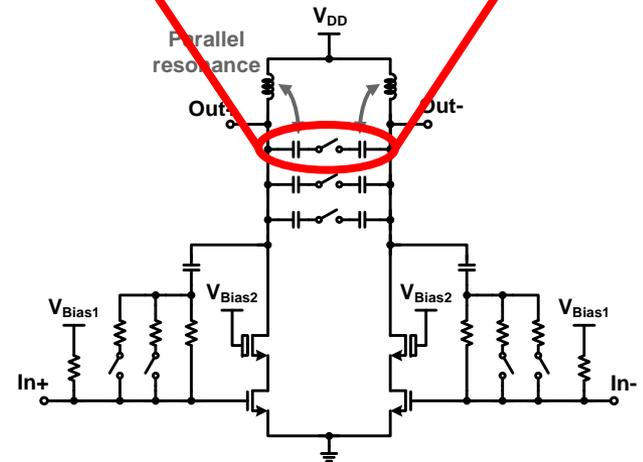
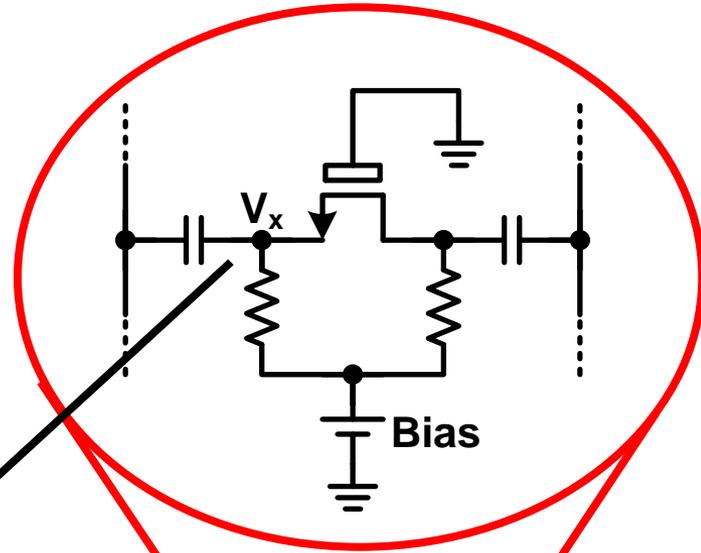
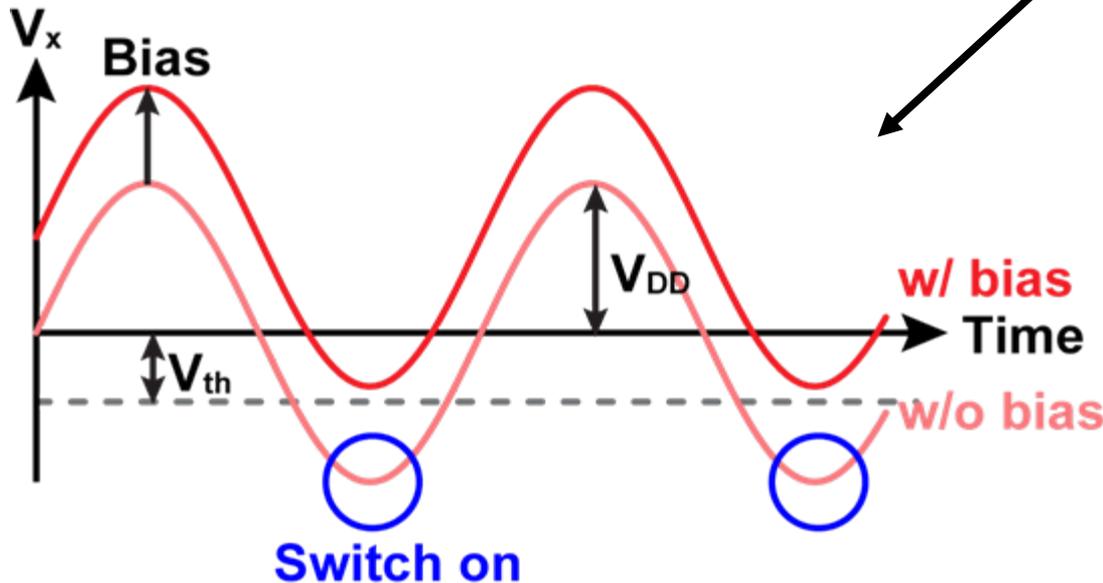


# Switch biasing

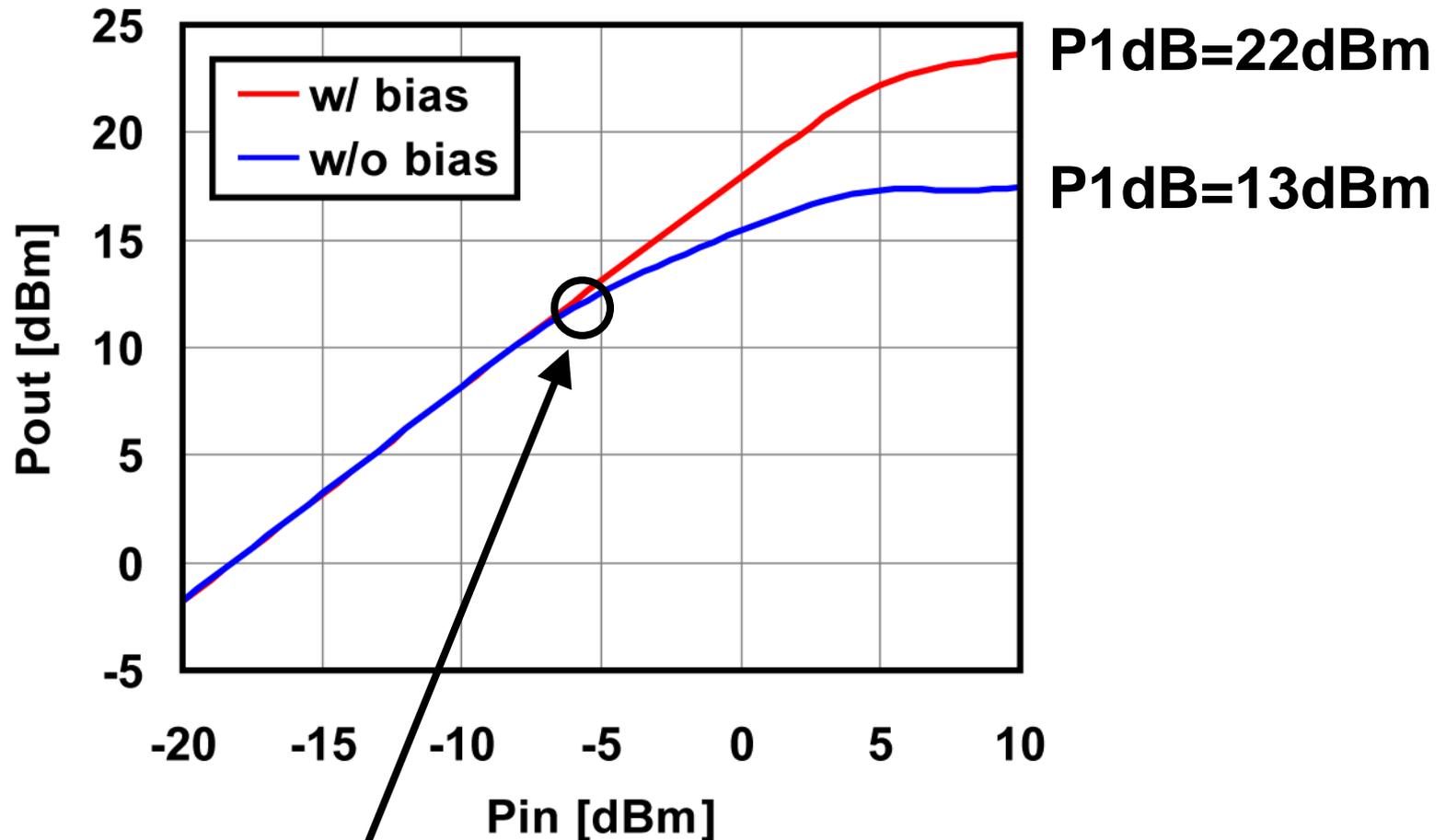
- Large voltage swing makes an off-state switch turned on for a moment
- Degrade large signal characteristics such as  $P_{1dB}$



Bias to source and drain of off-state switches



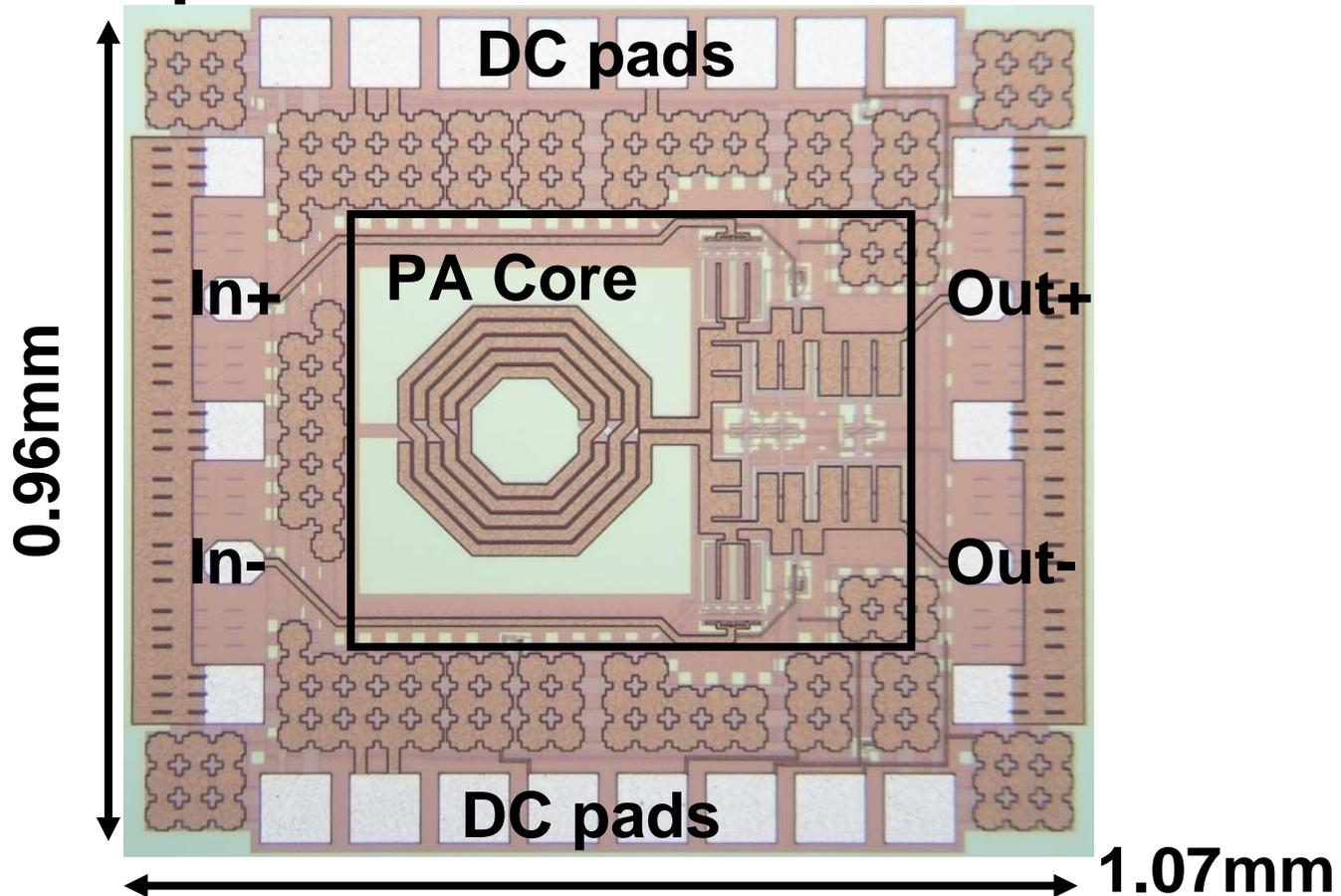
# Simulation of switch biasing effect



**Off-state switches start to be turned on**

# Chip micrograph[7]

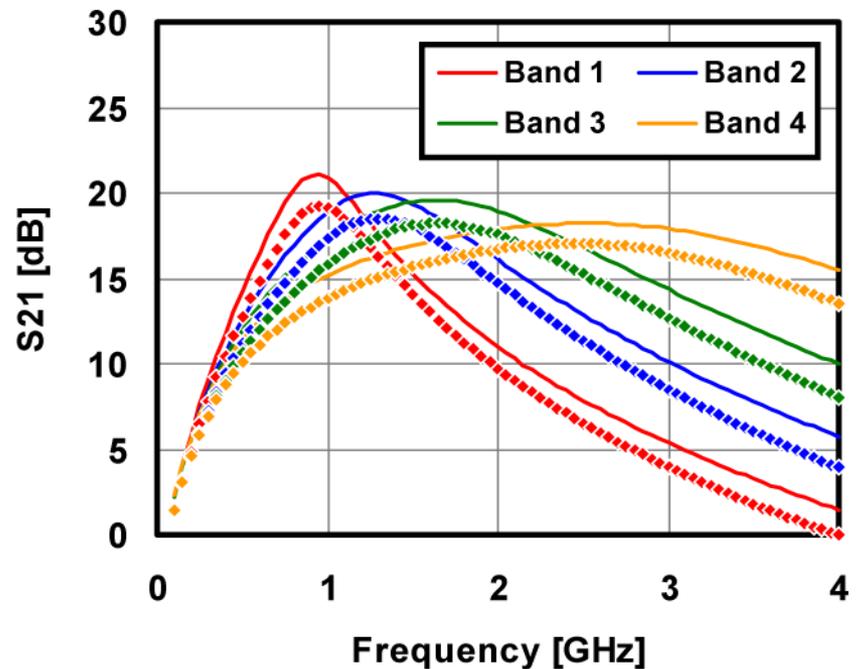
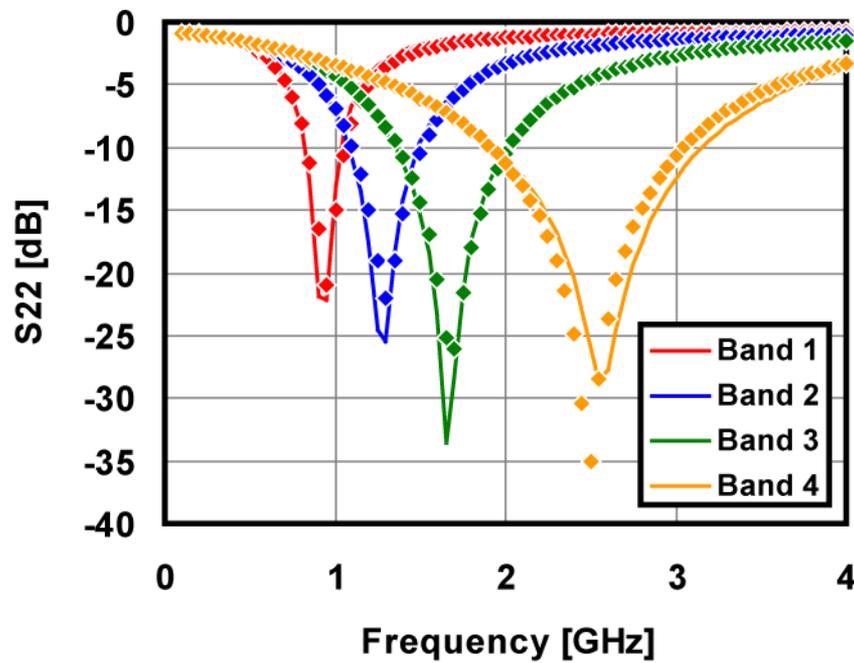
- 0.18 $\mu\text{m}$  CMOS
- Chip was measured using probes and external DC block capacitors



# Small signal S-parameters

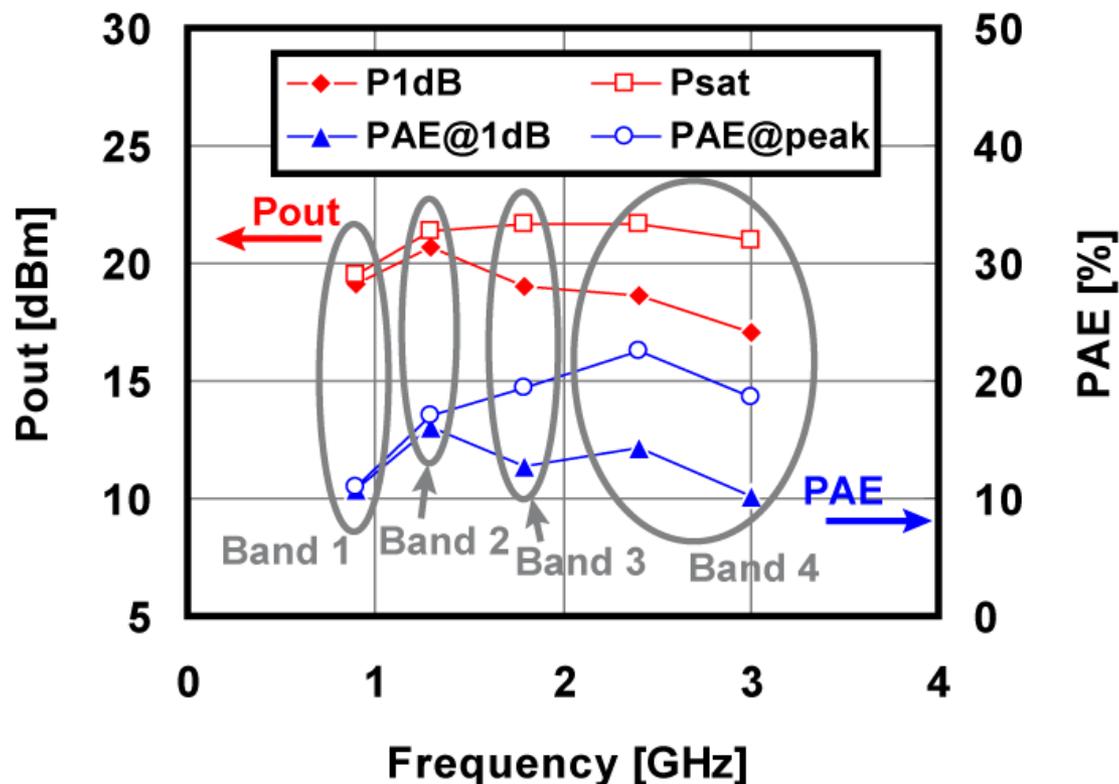
- Differential mode S-parameter calculated from 4-port S-parameter

Solid line : Simulation  
Marker : Measurement



**0.9~3.0GHz,  $S_{22} < -10\text{dB}$ ,  $S_{21} > 16\text{dB}$**

# $P_{out}$ , PAE v.s. Frequency



- Measured large signal performance in each band and each signal frequency
- $P_{sat}$  is larger than 19dBm, and PAE@peak is larger than 11% at the entire frequency range

# Comparison of CMOS PAs

	Tech.	$V_{DD}$ [V]	Freq. [GHz]	$P_{sat}$ [dBm]	PAE@peak [%]	Area [mm <sup>2</sup> ]	Output matching
RFIC '04 [3]	0.13 $\mu$ m CMOS	2.0	2.0 ~ 8.0	7 ~ 10	2 (@1dB)	—	Wideband
ISSCC '09 [4]	0.13 $\mu$ m CMOS	1.5	0.5 ~ 5.0	14 ~ 21	3 ~ 16 (drain eff.)	3.6	Wideband
T-MTT '07 [5]	0.18 $\mu$ m CMOS	2.8	3.7 ~ 8.8	16 ~ 19	8 ~ 25	2.8	Wideband
ISSCC '09 [6]	0.13 $\mu$ m CMOS	3.0	1.0 ~ 2.5	28 ~ 31	18 ~ 43	2.56*	Wideband
This work [7]	0.18 $\mu$ m CMOS	3.3	0.9 ~ 3.0	20 ~ 22	11 ~ 23	1.03	<b>Tunable</b>

\*With distributor

# Summary & Conclusion

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- **The first tunable CMOS PA utilizing a feedback technique**
- **0.9-3.0 GHz output matching**
- **At the entire frequency range, over 19dBm output power and over 11% PAE is achieved**

# Outline

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- Roadmap for multi-standard RFIC
- Rx requirements
  - Linearity & NF
- LO requirements
  - Q and  $V_{DD}$
  - Frequency tuning range
  - Multi-band VCO results
- Tx requirements
  - Tunable PA results
- **Conclusion**

# Conclusion

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## Rx

- **NF and linearity trade-off is very tough for realizing a full-SDR/CR. A new idea is still required.**
- **Some kind of reconfiguration is required to satisfy various requirements for every wireless standards.**
  - Linearity, Noise, Power consumption, etc
- **We should also pay attention to the research trend of external components, e.g., duplexer, antenna, SW, etc.**

## Tx

- **Tunability is required.**

## LO

- **There are some ways, but it is still challenging.**

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4. J. Roderick and H. Hashemi, "A 0.13 m CMOS Power Amplifier with Ultra-Wide Instantaneous Bandwidth for Imaging Applications," IEEE International Solid-State Circuits Conference, pp.374-375, Feb. 2009.

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## Rx

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# Appendix

# 3GPP standard (GSM/UMTS/LTE)

E-UTRA Operating Band	Uplink (UL) operating band BS receive UE transmit $F_{UL\_low} - F_{UL\_high}$	Downlink (DL) operating band BS transmit UE receive $F_{DL\_low} - F_{DL\_high}$	Duplex Mode	Tx-Rx separation	Band width	
1	1920 MHz – 1980 MHz	2110 MHz – 2170 MHz	FDD	190 MHz	60 MHz	UMTS2100 (Japan)
2	1850 MHz – 1910 MHz	1930 MHz – 1990 MHz	FDD	80 MHz	60 MHz	PCS/DCS1900(region2 North America)
3	1710 MHz – 1785 MHz	1805 MHz – 1880 MHz	FDD	95 MHz	75 MHz	DCS/GSM1800 (EU, China, etc)
4	1710 MHz – 1755 MHz	2110 MHz – 2155 MHz	FDD	400 MHz	45 MHz	UMTS1.7/2.1 (AWS, region 2)
5	824 MHz – 849 MHz	869 MHz – 894 MHz	FDD	45 MHz	25 MHz	UMTS850 (GSM850, region 2)
6	830 MHz – 840 MHz	875 MHz – 885 MHz	FDD	45 MHz	10 MHz	UMTS800 (Japan)
7	2500 MHz – 2570 MHz	2620 MHz – 2690 MHz	FDD	120 MHz	70 MHz	UMTS2600 (North America)
8	880 MHz – 915 MHz	925 MHz – 960 MHz	FDD	45 MHz	35 MHz	UMTS900 (E-GSM900) (EU, China, etc)
9	1749.9 MHz – 1784.9 MHz	1844.9 MHz – 1879.9 MHz	FDD	95 MHz	35 MHz	UMTS1700 (Japan)
10	1710 MHz – 1770 MHz	2110 MHz – 2170 MHz	FDD	400 MHz	60 MHz	Extended UMTS1.7/2.1 (region 2)
11	1427.9 MHz – 1452.9 MHz	1475.9 MHz – 1500.9 MHz	FDD	48 MHz	25 MHz	UMTS1500 (Japan, PDC1500)
12	698 MHz – 716 MHz	728 MHz – 746 MHz	FDD	30 MHz	18 MHz	TBD
13	777 MHz – 787 MHz	746 MHz – 756 MHz	FDD	-31 MHz	10 MHz	TBD
14	788 MHz – 798 MHz	758 MHz – 768 MHz	FDD	-30 MHz	10 MHz	TBD
...						
17	704 MHz – 716 MHz	734 MHz – 746 MHz	FDD	30 MHz	12 MHz	TBD
18	815 MHz – 830 MHz	860 MHz – 875 MHz	FDD	45 MHz	15 MHz	TBD
19	830 MHz – 845 MHz	875 MHz – 890 MHz	FDD	45 MHz	15 MHz	TBD
...						
33	1900 MHz – 1920 MHz	1900 MHz – 1920 MHz	TDD		20 MHz	
34	2010 MHz – 2025 MHz	2010 MHz – 2025 MHz	TDD		15 MHz	
35	1850 MHz – 1910 MHz	1850 MHz – 1910 MHz	TDD		60 MHz	
36	1930 MHz – 1990 MHz	1930 MHz – 1990 MHz	TDD		60 MHz	
37	1910 MHz – 1930 MHz	1910 MHz – 1930 MHz	TDD		20 MHz	
38	2570 MHz – 2620 MHz	2570 MHz – 2620 MHz	TDD		50 MHz	
39	1880 MHz – 1920 MHz	1880 MHz – 1920 MHz	TDD		40 MHz	
40	2300 MHz – 2400 MHz	2300 MHz – 2400 MHz	TDD		100 MHz	

3GPP TS 36.101, v9.1.0, 2009-09

+ GPS, DTV, WLAN, Bluetooth

# Theoretical limit of phase noise

	NMOS VCO	CMOS VCO	Class-C VCO
$v_{out+}, v_{out-}$	$0 \sim 2V_{DD}$	$0 \sim V_{DD}$	$V_{DD} \pm \frac{V_{DD}+V_{od}}{1+k}$
$v_{sig}$	$R_p i_{sig}$	$R_p i_{sig}$	$R_p i_{sig}$
$i_{sig}$	$\frac{2}{\pi} I_{bias} \sin \omega t$	$\frac{4}{\pi} I_{bias} \sin \omega t$	$I_{bias} \sin \omega t$
I-limit	$I_{bias} < \frac{\pi V_{DD}}{R_p}$	$I_{bias} < \frac{\pi V_{DD}}{4R_p}$	$\frac{V_{od}}{kR_p} < I_{bias} < \frac{V_{DD}+V_{od}}{(1+k)R_p}$
$P_{sig(I \text{ region})}$	$\frac{2R_p I_{bias}^2}{\pi^2}$	$\frac{8R_p I_{bias}^2}{\pi^2}$	$\frac{R_p I_{bias}^2}{2}$
$P_{sig(V \text{ region})}$	$\frac{2V_{DD}^2}{R_p}$	$\frac{V_{DD}^2}{2R_p}$	—
$P_{sig(max)}$	$\frac{2V_{DD}^2}{R_p}$	$\frac{V_{DD}^2}{2R_p}$	$\frac{1}{2R_p} \left( \frac{V_{DD}+V_{od}}{1+k} \right)^2$
$PN_{(I \text{ region})}$	$\frac{f_0^2}{\Delta f^2} \frac{k_B T}{Q^2} \frac{\pi^2(1+\gamma_N)}{4R_p I_{bias}^2}$	$\frac{f_0^2}{\Delta f^2} \frac{k_B T}{Q^2} \frac{\pi^2(1+\frac{\gamma_N+\gamma_P}{2})}{16R_p I_{bias}^2}$	$\frac{f_0^2}{\Delta f^2} \frac{k_B T}{Q^2} \frac{(1+\frac{\gamma_N}{k})}{2R_p I_{bias}^2}$
$PN_{(V \text{ region})}$	$\frac{f_0^2}{\Delta f^2} \frac{k_B T}{Q^2} \frac{(1+\gamma_N)R_p}{4V_{DD}^2}$	$\frac{f_0^2}{\Delta f^2} \frac{k_B T}{Q^2} \frac{(1+\frac{\gamma_N+\gamma_P}{2})R_p}{V_{DD}^2}$	—
$PN_{(min)}$	$\frac{f_0^2}{\Delta f^2} \frac{k_B T}{Q^2} \frac{(1+\gamma_N)R_p}{4V_{DD}^2}$	$\frac{f_0^2}{\Delta f^2} \frac{k_B T}{Q^2} \frac{(1+\frac{\gamma_N+\gamma_P}{2})R_p}{V_{DD}^2}$	$\frac{f_0^2}{\Delta f^2} \frac{k_B T}{Q^2} \frac{(1+\frac{\gamma_N}{k})R_p(1+k)^2}{2(V_{DD}+V_{od})^2}$
$FoM_{(I \text{ region})}$	$\frac{10^3 k_B T}{Q^2} \frac{\pi^2(1+\gamma_N)V_{DD}}{4R_p I_{bias}}$	$\frac{10^3 k_B T}{Q^2} \frac{\pi^2(1+\frac{\gamma_N+\gamma_P}{2})V_{DD}}{16R_p I_{bias}}$	$\frac{10^3 k_B T}{Q^2} \frac{(1+\frac{\gamma_N}{k})V_{DD}}{2R_p I_{bias}}$
$FoM_{(V \text{ region})}$	$\frac{10^3 k_B T}{Q^2} \frac{(1+\gamma_N)R_p I_{bias}}{4V_{DD}}$	$\frac{10^3 k_B T}{Q^2} \frac{(1+\frac{\gamma_N+\gamma_P}{2})R_p I_{bias}}{V_{DD}}$	—
$FoM_{(min)}$	$\frac{10^3 k_B T}{Q^2} \frac{\pi(1+\gamma_N)}{4}$	$\frac{10^3 k_B T}{Q^2} \frac{\pi(1+\frac{\gamma_N+\gamma_P}{2})}{4}$	$\frac{10^3 k_B T}{Q^2} \frac{(1+\frac{\gamma_N}{k})(1+k)V_{DD}}{2(V_{DD}+V_{od})}$