A Comparison Between Varactor-DAC and Capacitor-Bank DCOs

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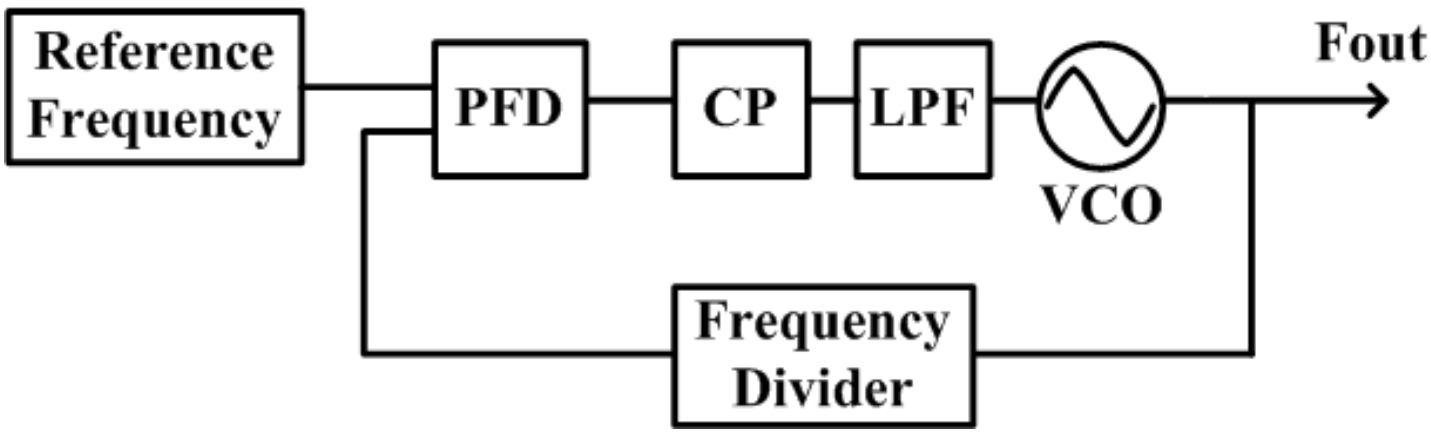
Introduction

- VCO output frequency cannot be accurately predicted.
- A PLL is used to automatically adjust the VCO.
- Most used type is CPPLL.
- Recently ADPLL is gaining more popularity.



General PLL Architecture

ADPLL

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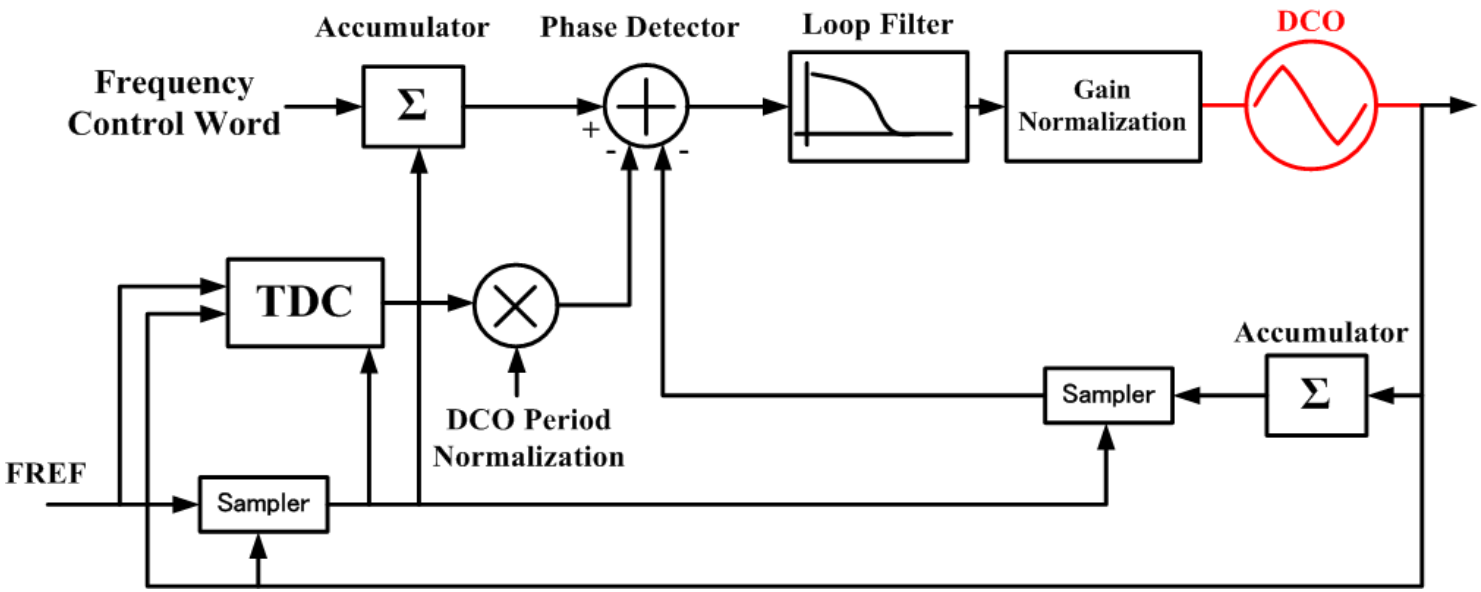
- ADPLL has many advantages over CPPLL.
  - Loop bandwidth can be easily changed on the fly.
  - Intermediate signals can be monitored in real time.
  - DSP can be used to improve performance.
- Digitally Controlled Oscillator is the main part of ADPLL.



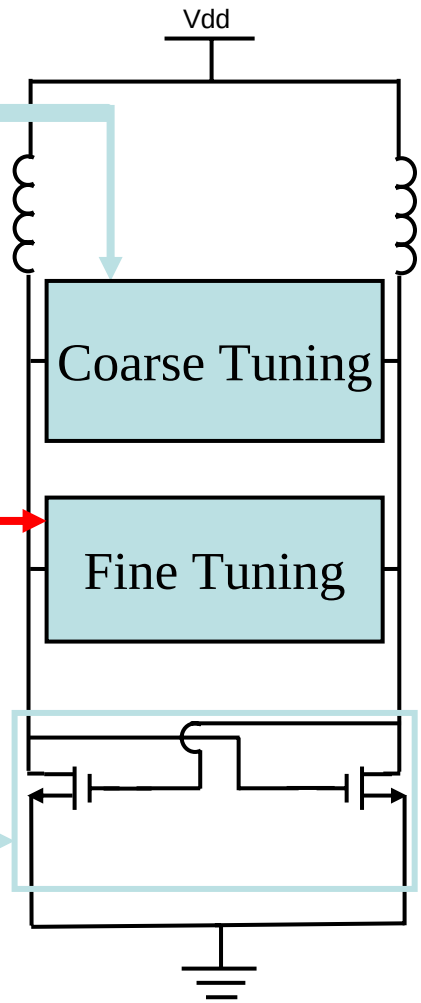
W. Chaivipas, P. Oh, and A. Matsuzawa, "All-DigitalPhase-Locked Loops, its Advantages and Performance Limitations", International PhD student Workshop, Jul. 2006.

DCO Structure

- Used for channel selection.
- Relatively large size switches and capacitors.
- Only few are needed.

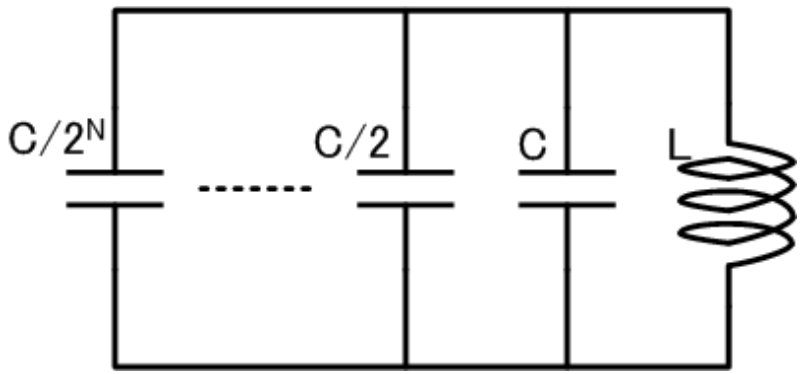
- Used for frequency tuning within a channel.
- Fine steps are required.

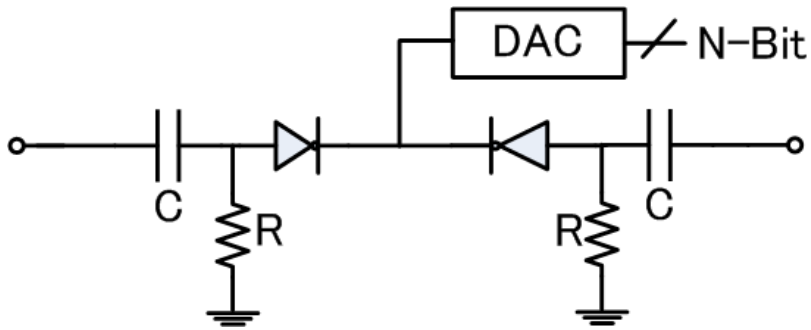
- Negative *gm* cell to compensate for the losses in the tank circuit.



DCO's Fine Tuning

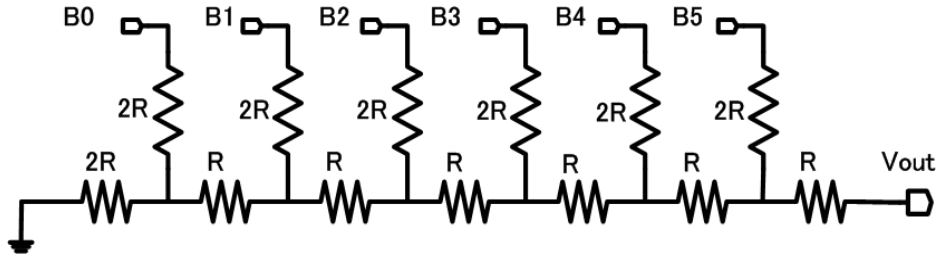
- Issues with the DCO:
  - A lot of capacitors are required to provide fine continuous tuning.
  - Minimum frequency step.
    - Very small capacitors.
      - Parasitic problems.
- Varactor-DAC fine tuning.
  - Small area.
  - Resistor mismatch for higher resolution.

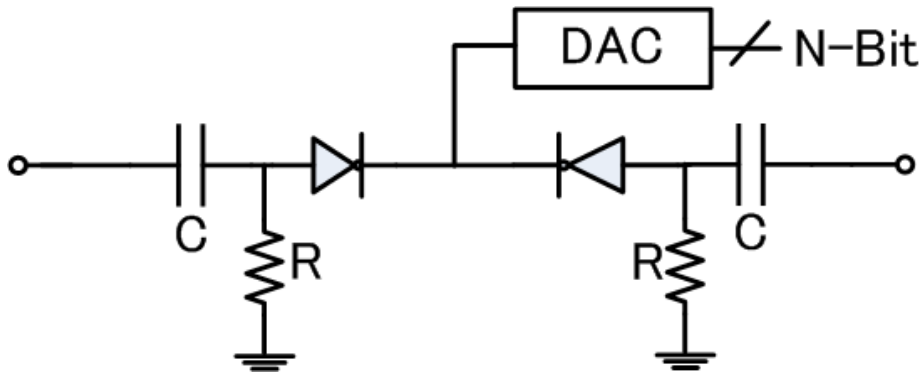




Varactor-DAC

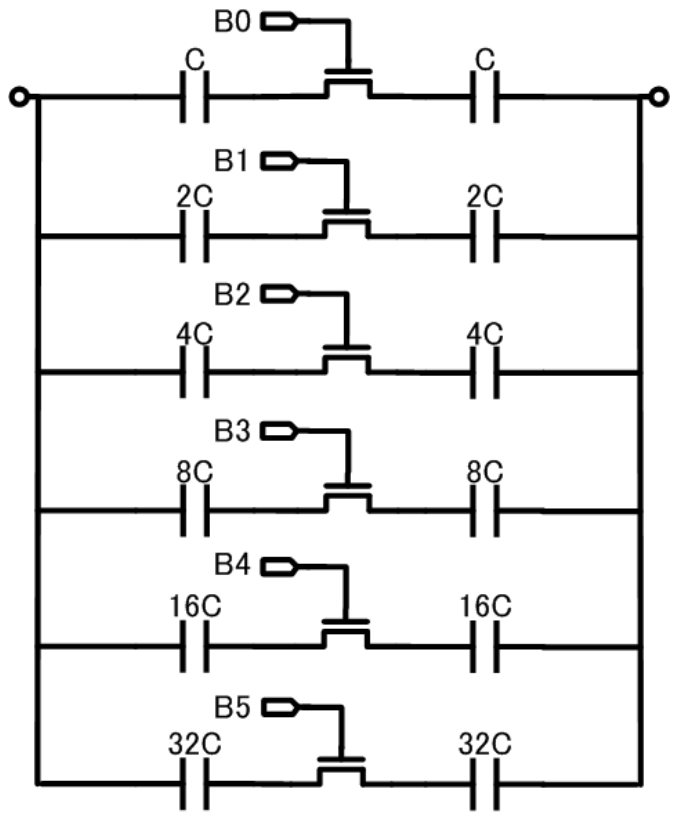
- A 6-bit R/2R ladder DAC was utilized.
- Varactor-DAC configuration is constructed with the following specifications:
  - C = 170 fF - 112 fF
  - Q = 32 - 40
  - R = 4.9 - 5.9 ohm
- Current Consumption of about 0.2mA.
- 0.34dB added noise



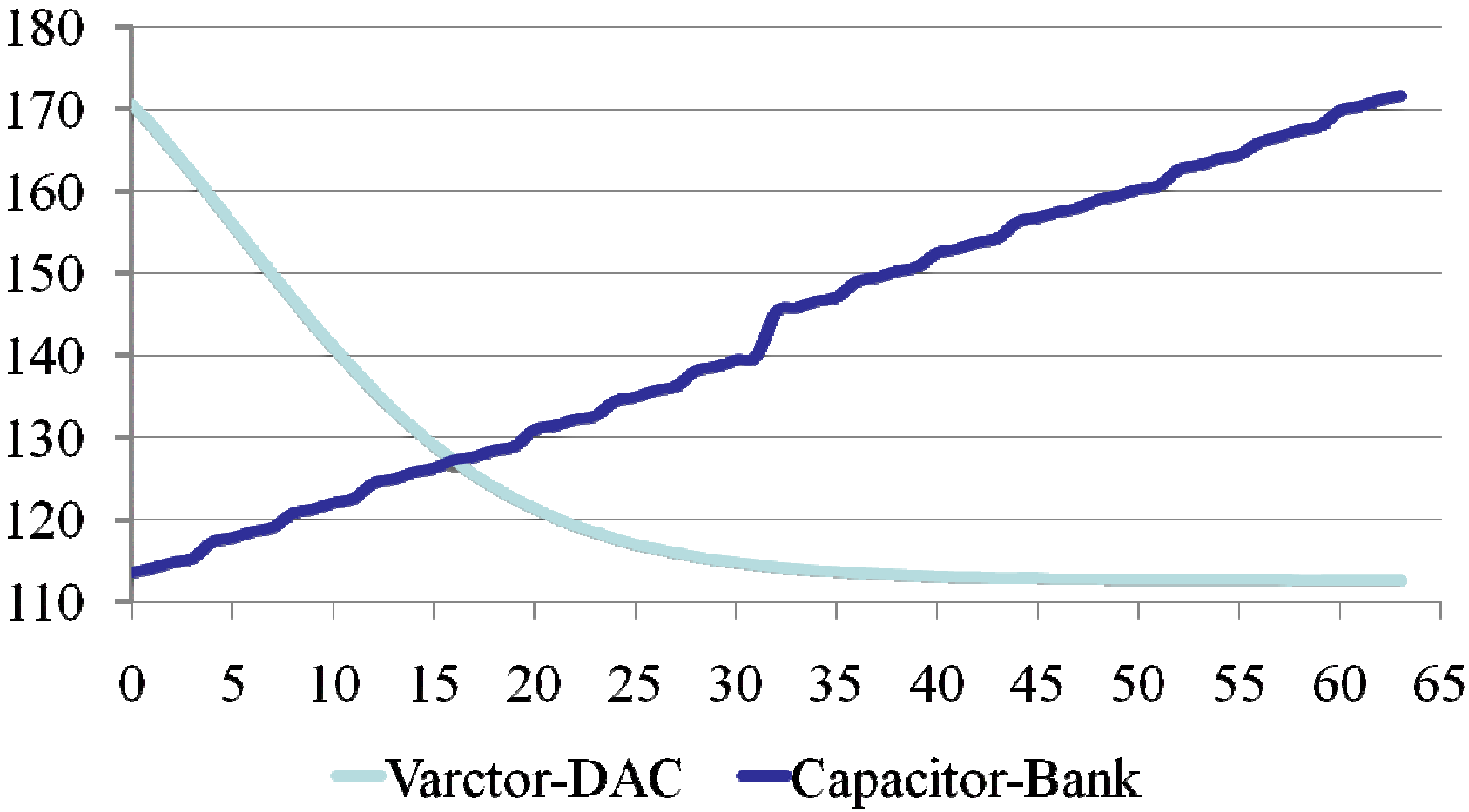


Capacitor-Bank

- 6 switches were used to construct a 6-bit switched capacitor-bank.
- The capacitor-bank has the following specification:
  - C = 171 fF - 113 fF
  - Q = 60.5 - 32
  - R = 3 - 8.8 ohm
- Both the varactor-DAC and the capacitor-bank were used to tune the same DCO.



Capacitance *vs.* Binary Code



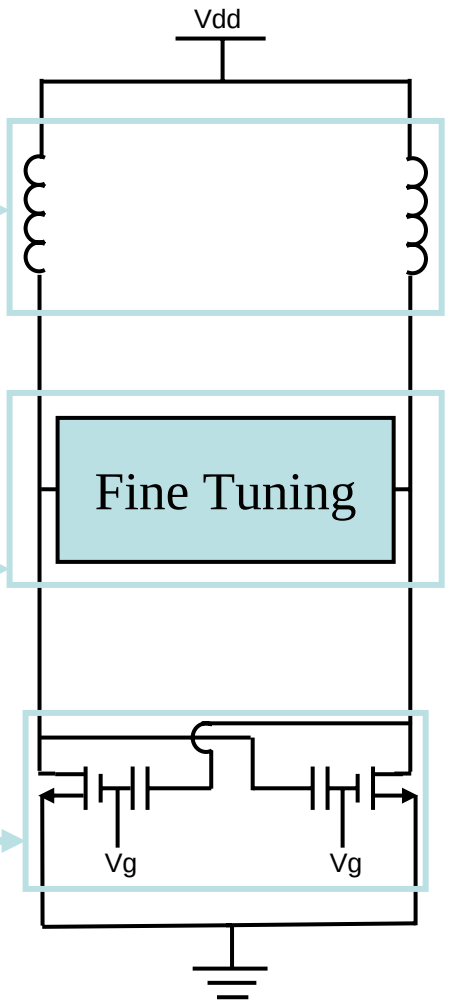
Simulation DCO Structure

- 0.18µm CMOS process
- VDD: 1.8V

- Number of turns: 3
- Track width: 15µm
- Radius: 70µm
- Q: 6.1 @ 6GHz

1. Varactor-DAC.
2. Capacitor-bank.

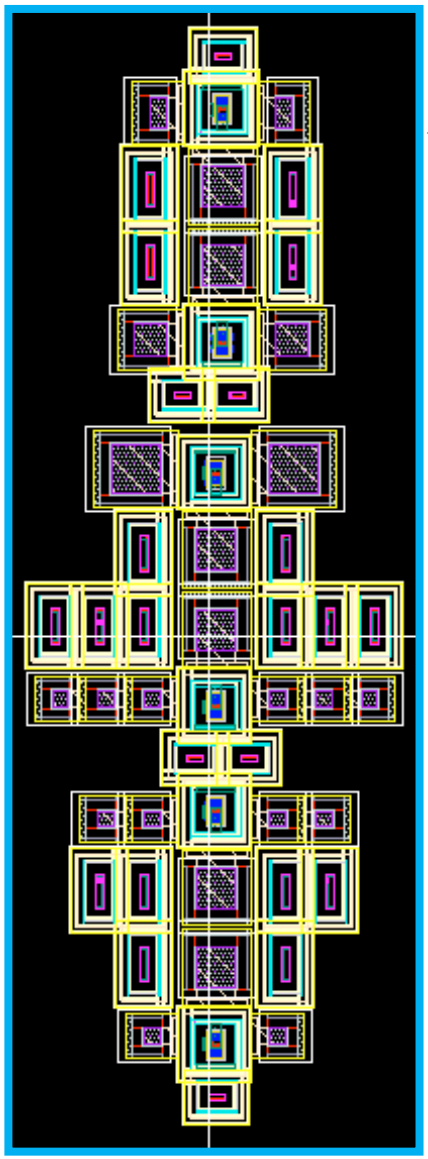
- L: 0.18µm
- W: 64µm
- Vg: 0.7 V



Simulation Results

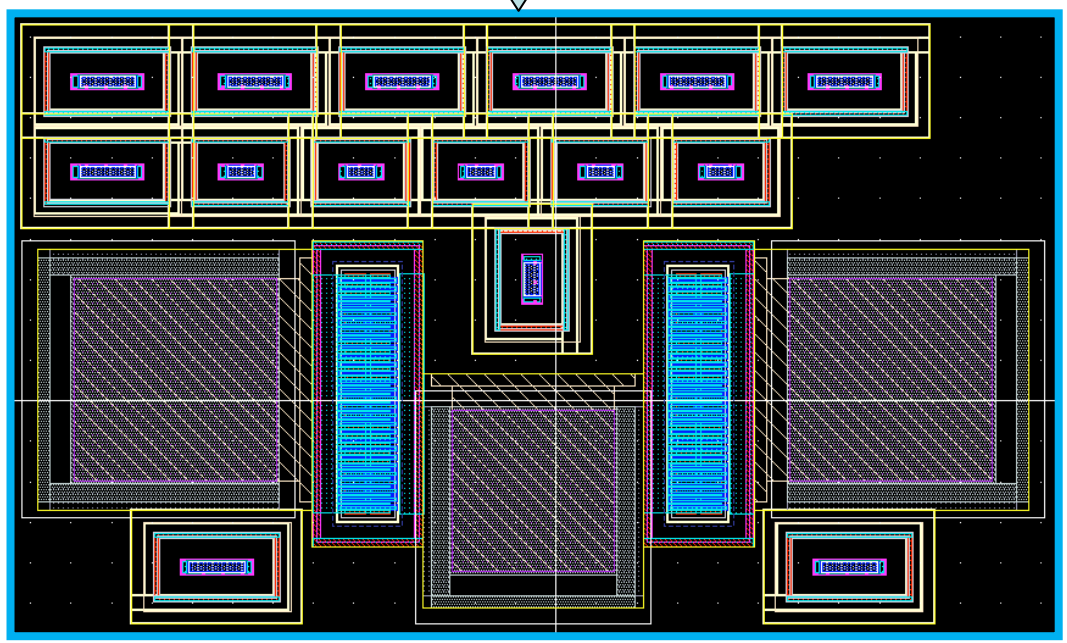
	Varactor-DAC	Capacitor-Bank
Frequency (GHz)	5.64 ~ 6.14	5.75 ~ 6.16
Tuning Range (MHz)	500	410
Minimum Step (MHz)	5.6 ~ 6.8	5.3
Phase Noise@ 1MHz (dBc/Hz)	109.8 ~ 110.4	108.4 ~ 117
FOM @ 1MHz	173.1 ~ 174.4	171.2 ~ 180.8
Layout Area (mm^2)	0.00938	0.02587
Current (mA)	8	7.7 ~ 11

Layout



Capacitor-bank
275µm X 95µm

Varactor-DAC
75µm X 127µm



Conclusion

- Using a varactor-DAC in fine tuning a DCO results in about 2.75 smaller area compared to using a capacitor bank.

- A capacitor-bank configuration has a better phase noise when all switches are on but a worse one when they are off.
- Increasing the resolution requires minimum components in the varactor-DAC configuration.

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Thank you!

Q & A!!