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Passive Device Characterization for 60-GHz CMOS Power Amplifiers

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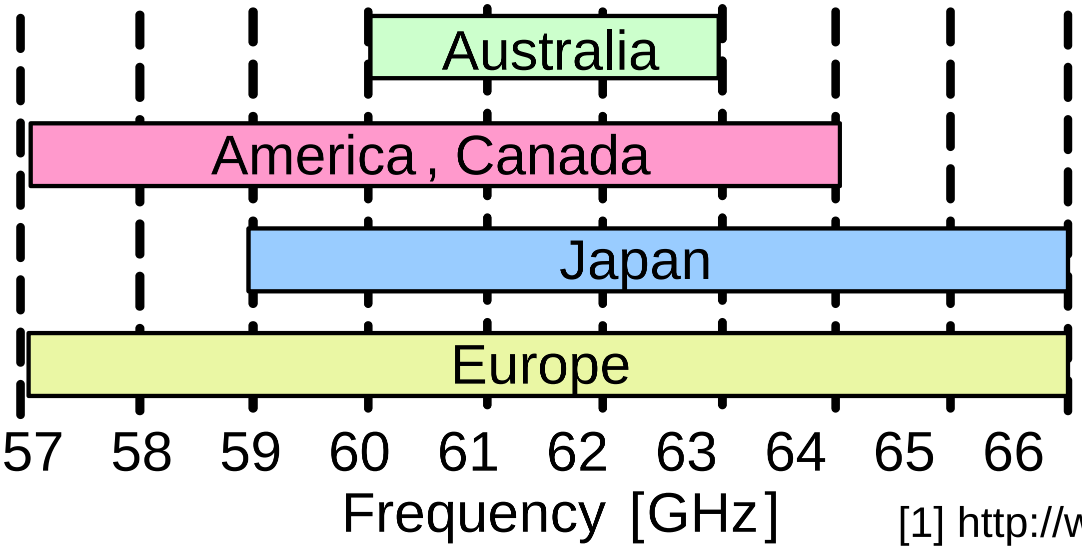
2009/4/20

Matsuzawa & Okada Lab.

Motivation

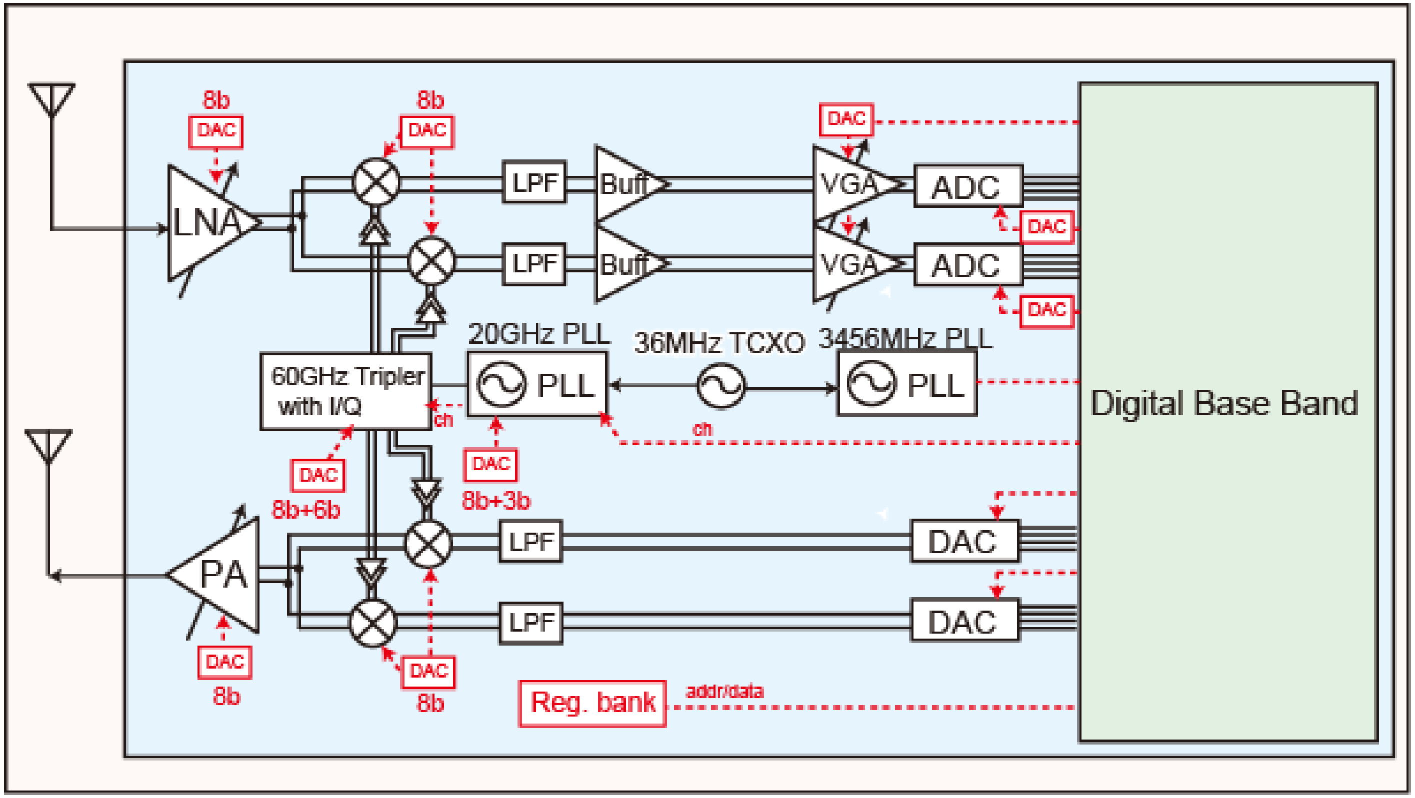
60GHz unlicensed band



[1] http://www.tele.soumu.go.jp

- 9GHz-BW around 60GHz
  ⇨ Several-Gbps wireless communication
- Use of CMOS process
  ⇨ Fab. cost is very important to generalize it.
  RF&BB mixed chip can be realized.

Our target



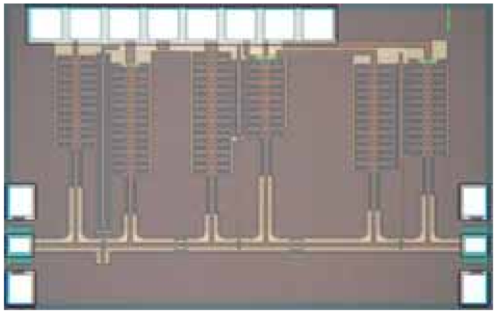
60GHz 2.16GHz-**full 4ch** direct-conversion by CMOS Tr

QPSK 3Gbps & **16QAM 6Gbps & 64QAM 9Gbps**

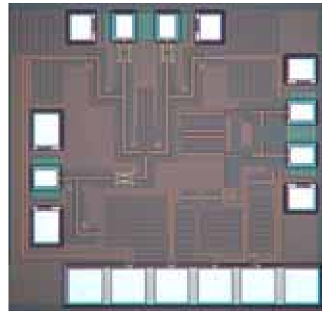
IEEE 802.15.3c conformance

Dynamic power management: <300mW for RF front-end

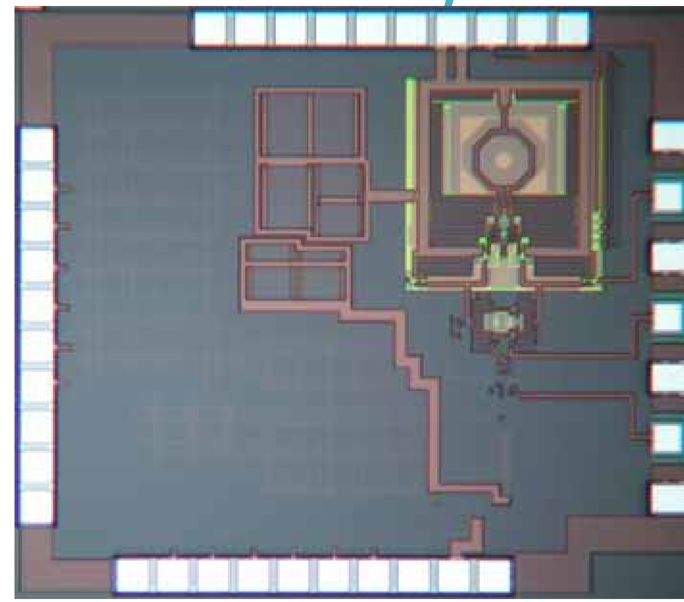
Circuit blocks of 60GHz transceiver



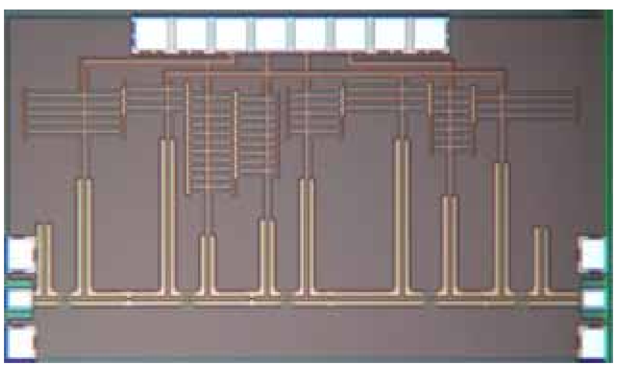
60GHz LNA



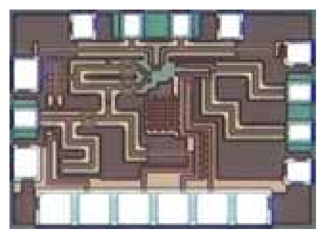
Down-Mixer



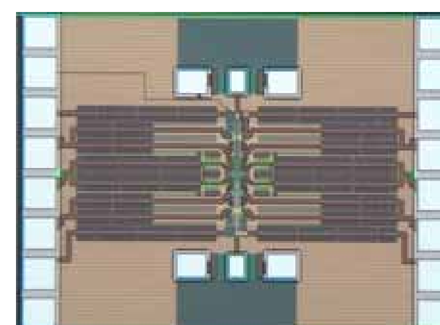
20GHz PLL



60GHz PA



Up-Mixer

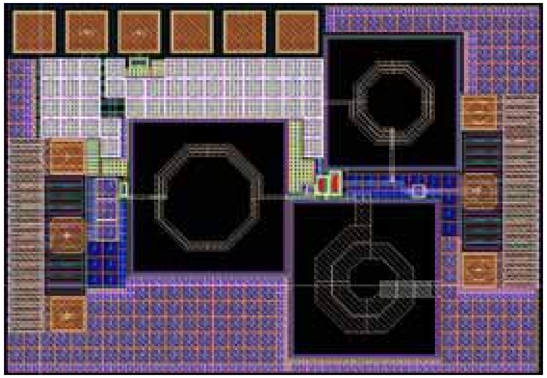


60GHz Tripler with quadrature output

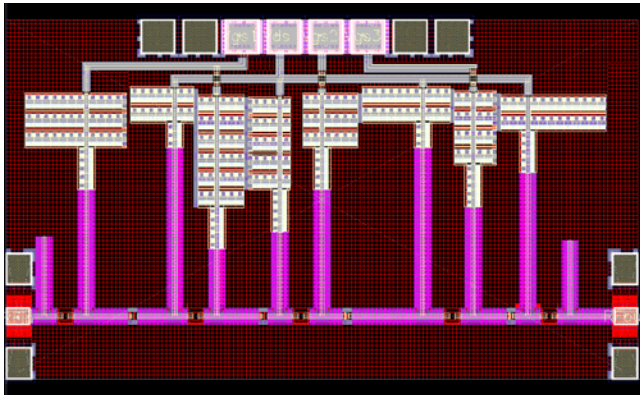
mmW CMOS circuit design

Matching is very important for mmw circuit design,
because (1) The wave length is very short,
(2) Tr's gain is very small, and
(3) Loss of TL is very large.

Matching blocks



Inductor@5GHz

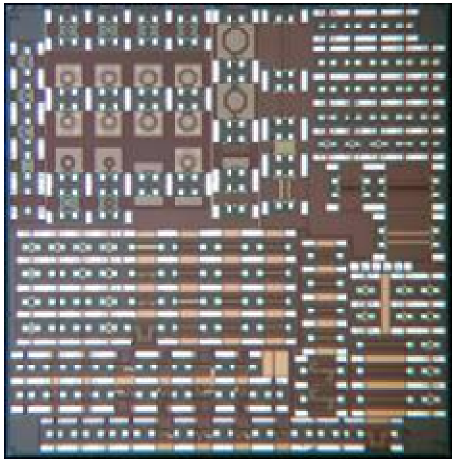


Transmission line@60GHz

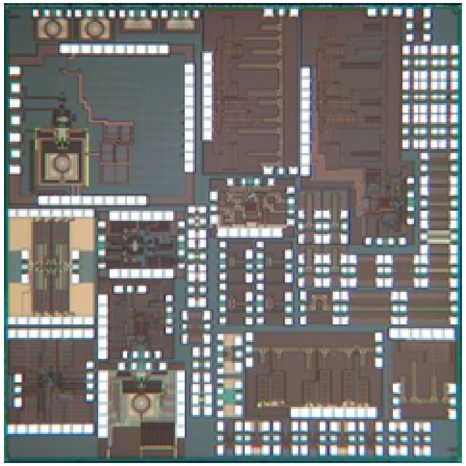
At 60GHz, every interconnects should be dealt with as a distributed component.

➡ The accurate characterization is required.

Overview of device characterization



Initial T.O.



Second T.O.

Initial T.O. for **Modeling**

- Transistors (CS, CG with various layouts)
- Transmission line (various length & Z_0)
- Branch & bend line
- Spiral inductor
- Balun
- Series capacitor
- Decoupling capacitor
- De-embedding patterns
- 1-stage amplifier for the model evaluation
- DC probe

Second T.O.

- Circuit building blocks
- Whole system

Overview of characterization

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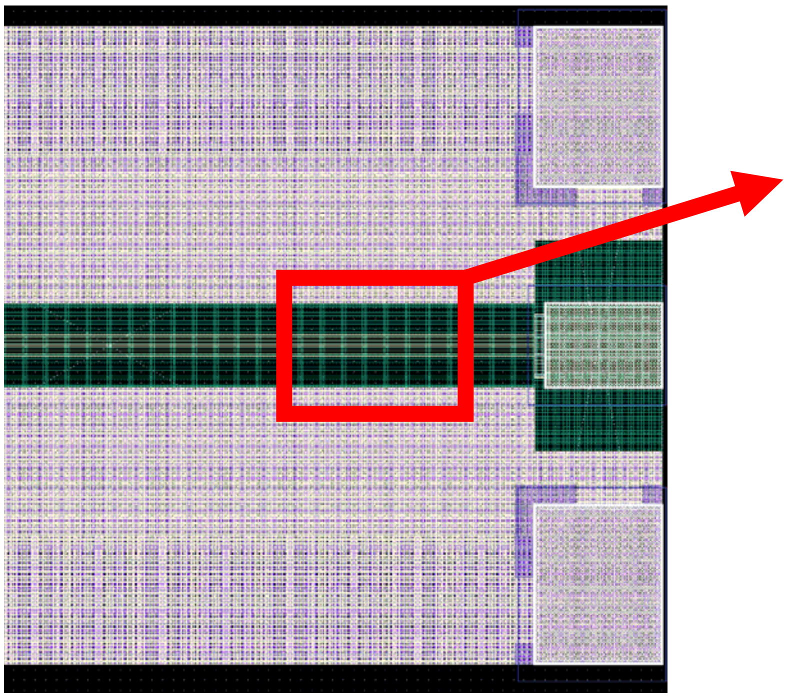
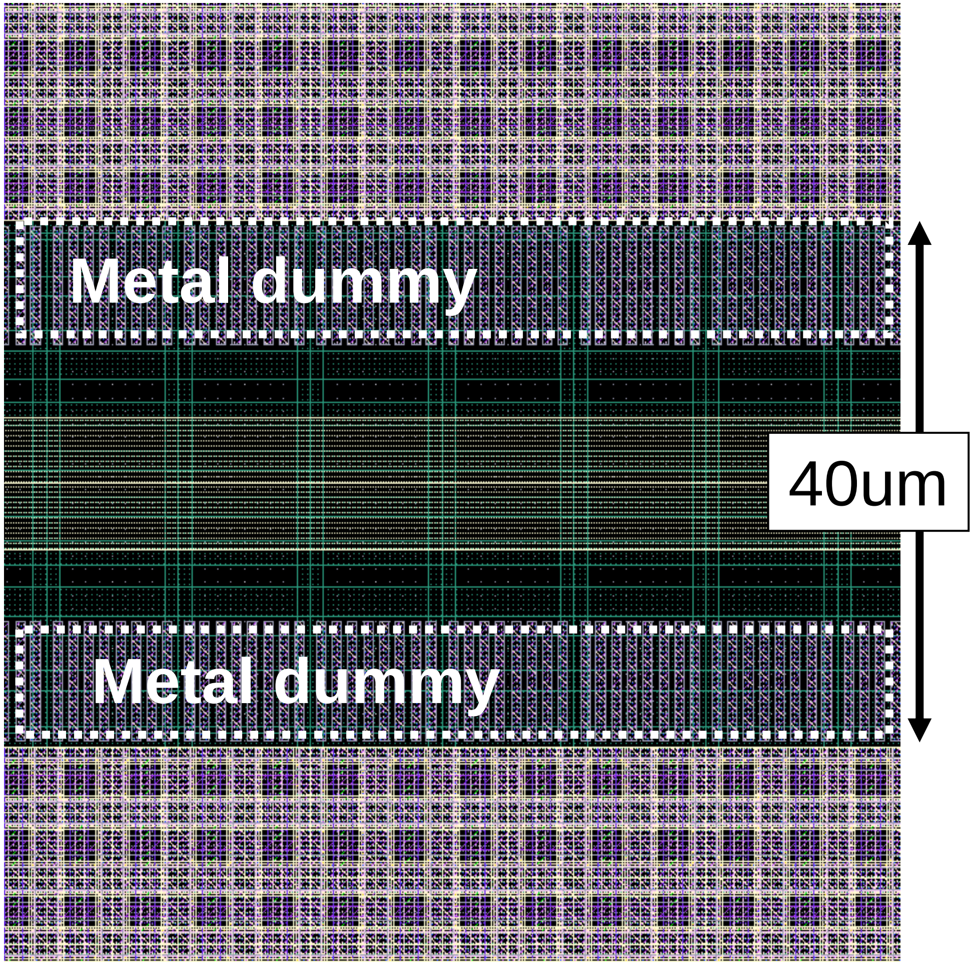
- Transmission line
- Branch & bend line
- Decoupling capacitor
- De-embedding patterns
- 1-stage amplifier
- DC probe
- 4-stage power amplifier

Dummy metal

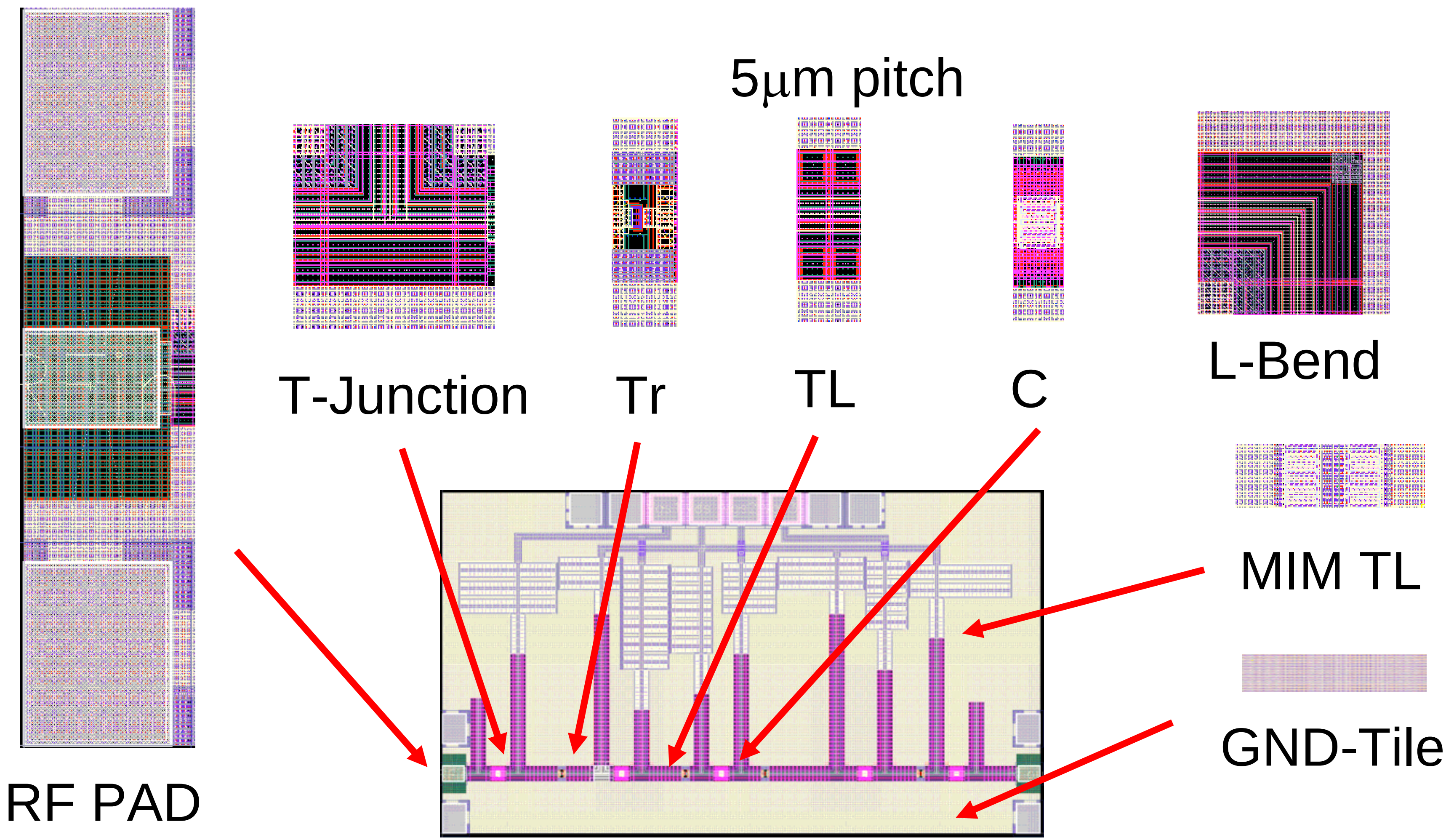
To avoid random production of dummy metal, it is manually placed to keep good reproducibility.





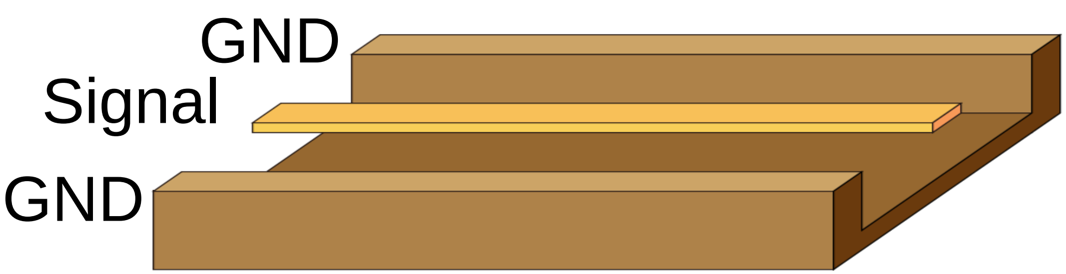
Tile-base layout

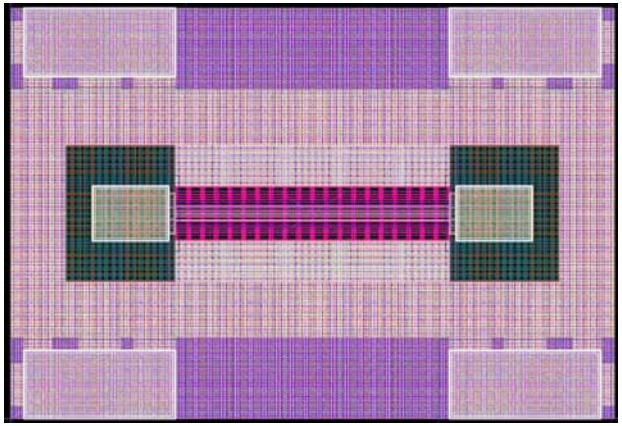
Each component is previously measured and modeled.
The same layout is utilized to maintain modeling accuracy.



Transmission line in CMOS chip

Guided microstrip line





$$e^{-\gamma\ell} = \left\{ \frac{1 - S_{11}{}^2 + S_{21}{}^2}{2S_{21}} \pm K \right\}^{-1}$$

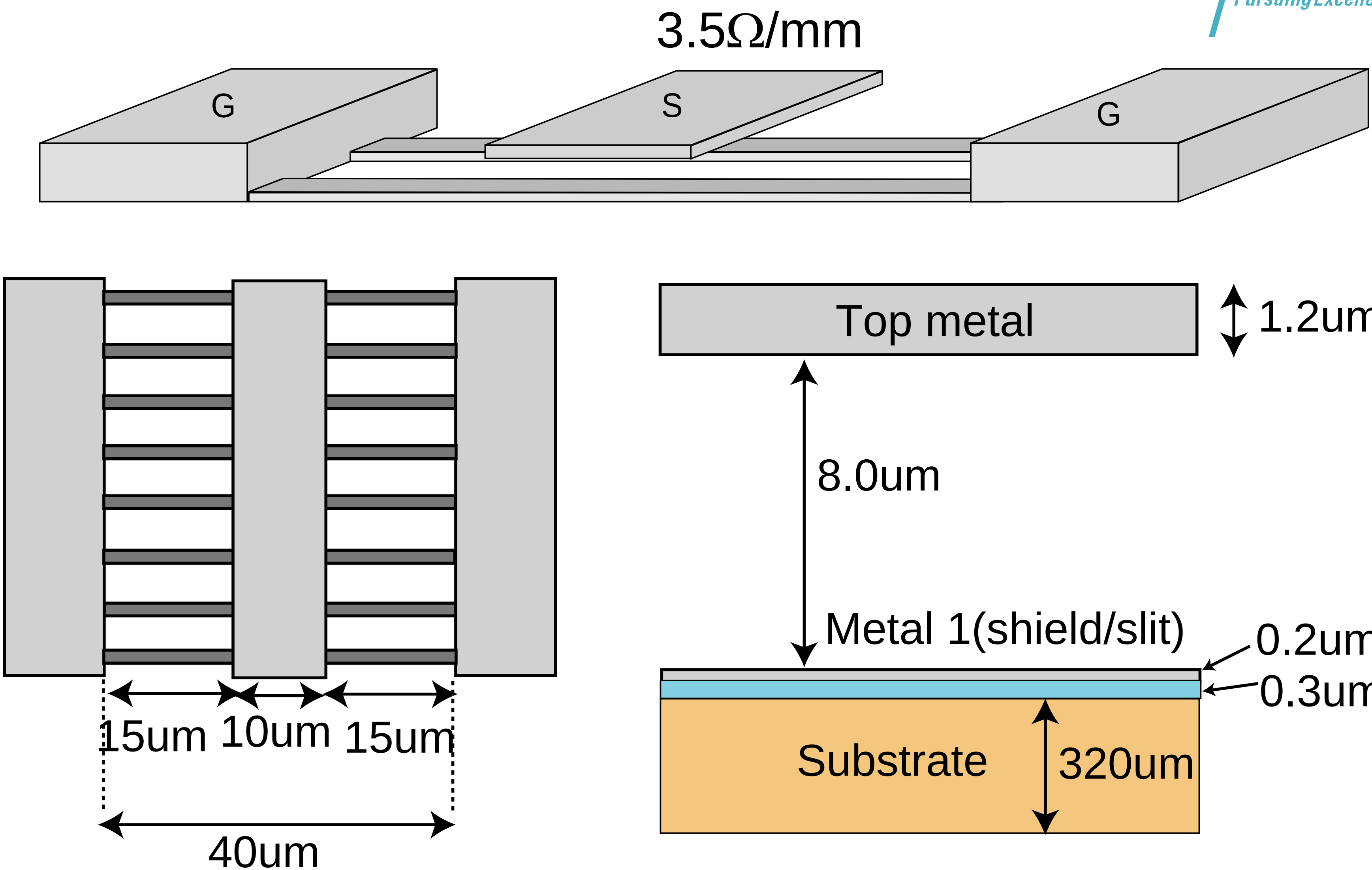
$$Z^2 = Z_0{}^2 \frac{(1 + S_{11})^2 - S_{21}{}^2}{(1 - S_{11})^2 - S_{21}{}^2}$$

$$K = \left\{ \frac{(S_{11}{}^2 + S_{21}{}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2} \right\}^{\frac{1}{2}}$$

$$\gamma = \alpha + j\beta$$

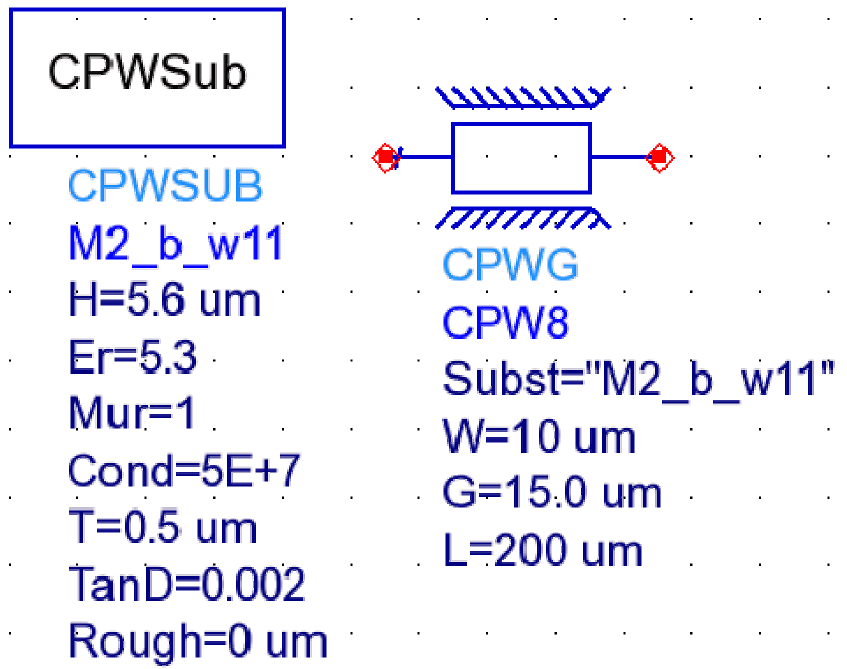
Slow-wave coplanar-waveguide is also utilized depending on a required characteristic impedance.

Cross-sectional structure



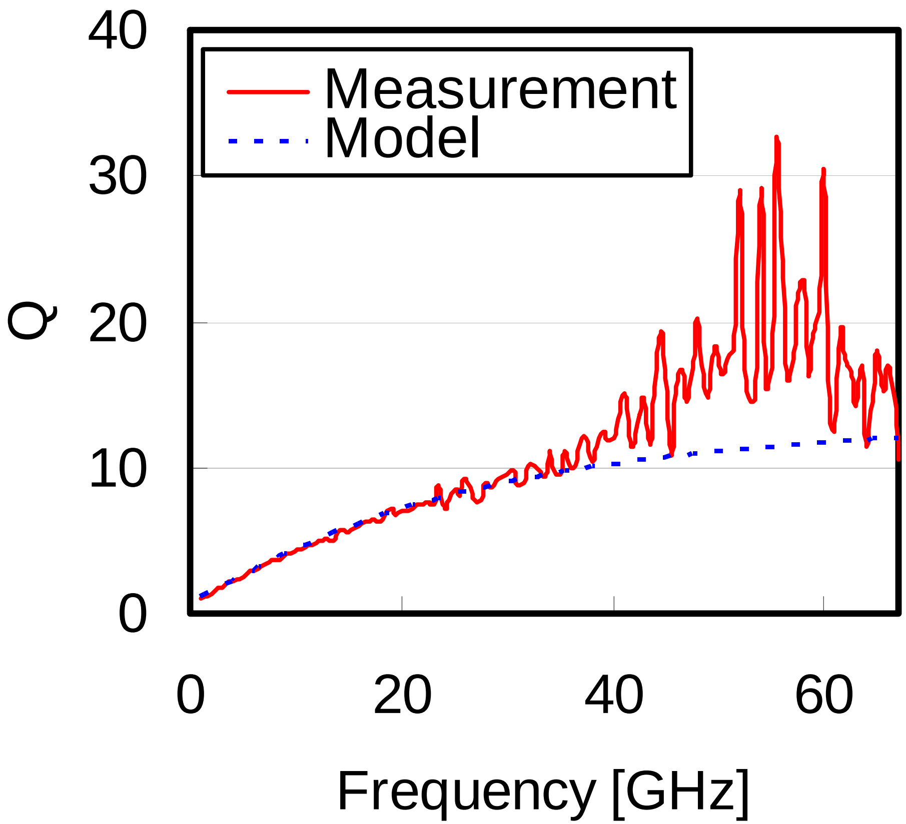
Modeling of transmission line

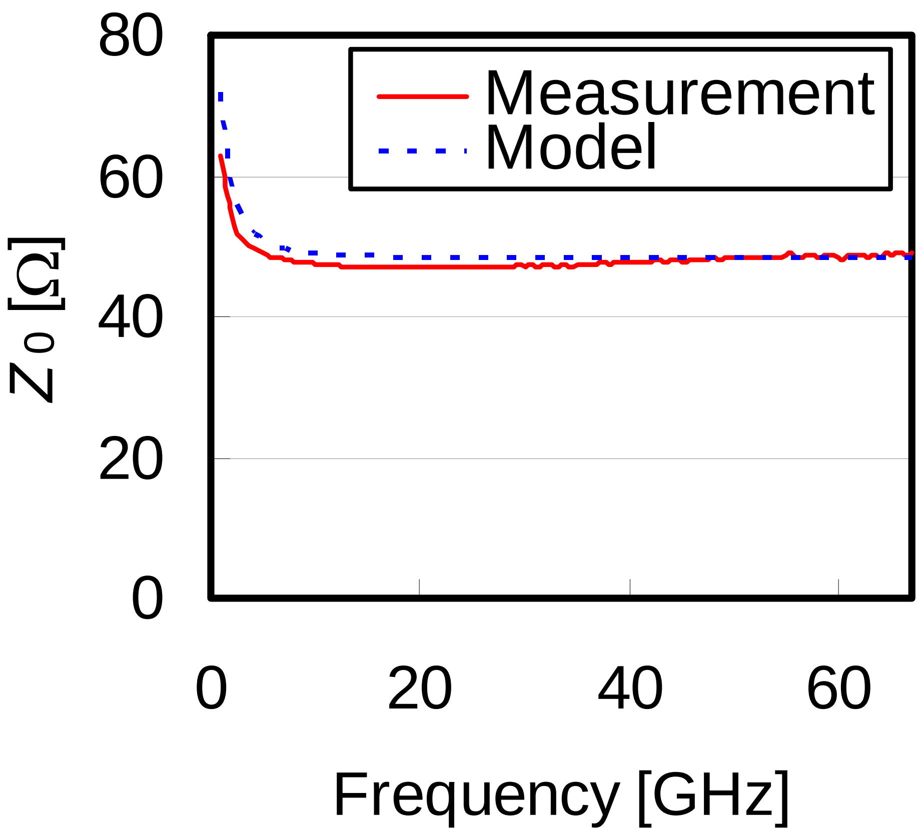
ADS's CPW model



To meet measured α, β, Q and Z_0, substrate model is individually extracted for each structure.

Transmission line (200μm)

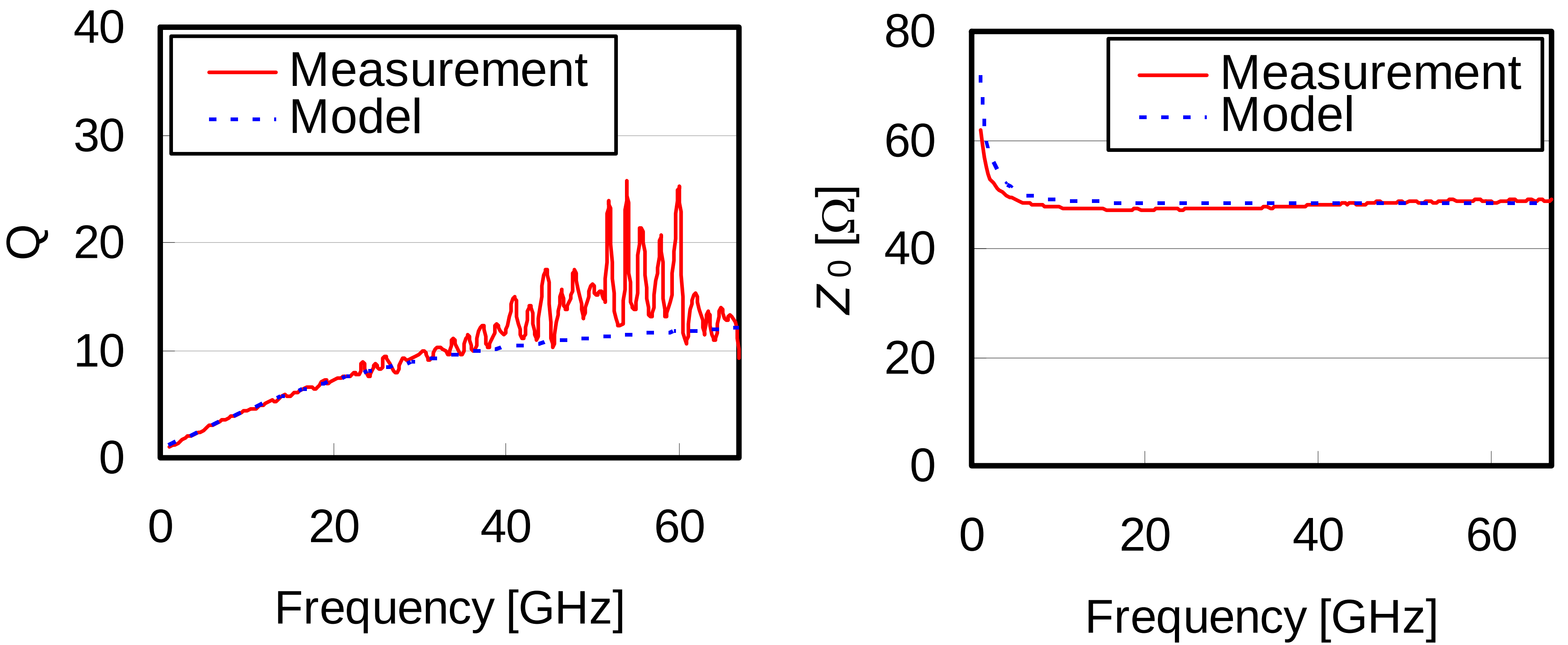




Improved Mangan's method is utilized with 200μm and 400μm transmission lines.

[2] A.M. Mangan, et al., IEEE Trans. on Electron Devices, vol. 53, no. 2, pp.235-241, Feb. 2006

Transmission line (400μm)

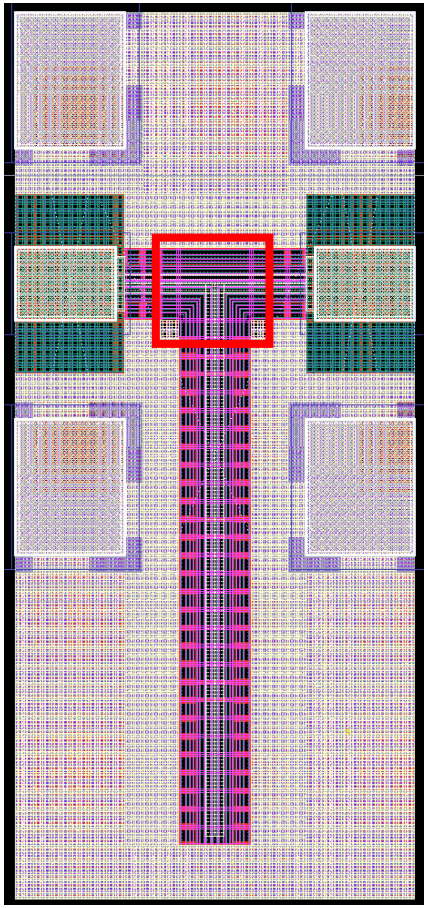


400μm of transmission line has almost the same characteristics with that of 200μm, which is a good proof of accurate modeling.

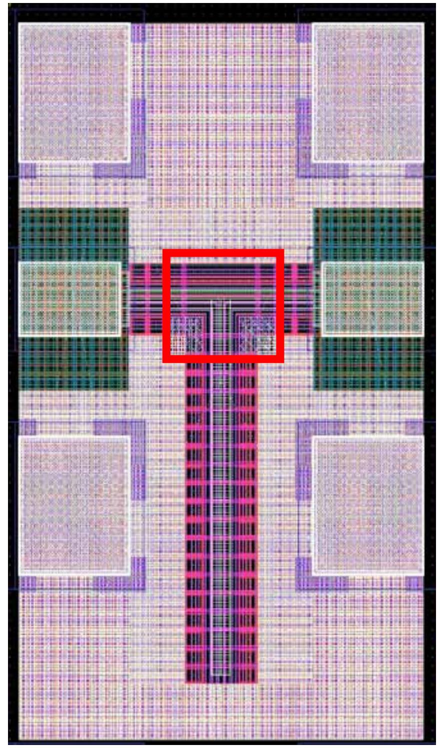
Overview of characterization

- Transmission line
- ➡ Branch & bend line
- Decoupling capacitor
- De-embedding patterns
- 1-stage amplifier
- DC probe
- 4-stage power amplifier

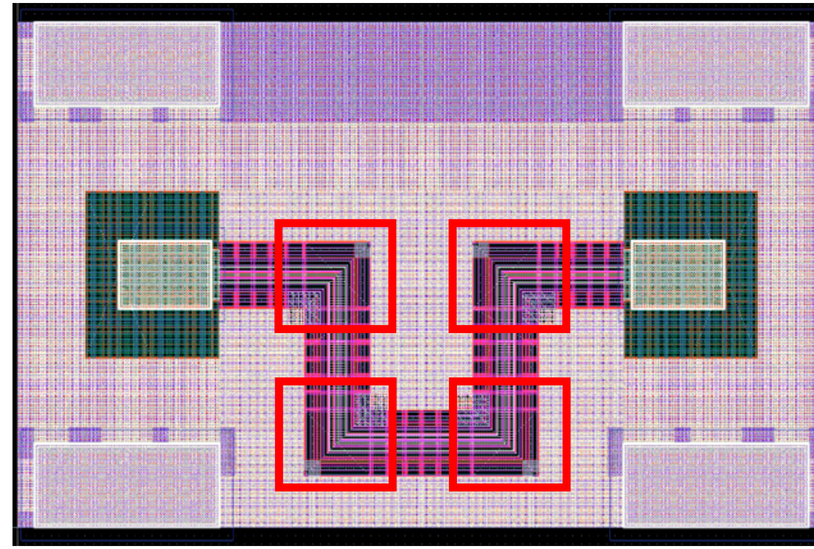
Branch & bend modeling



with 300μm shunt TL



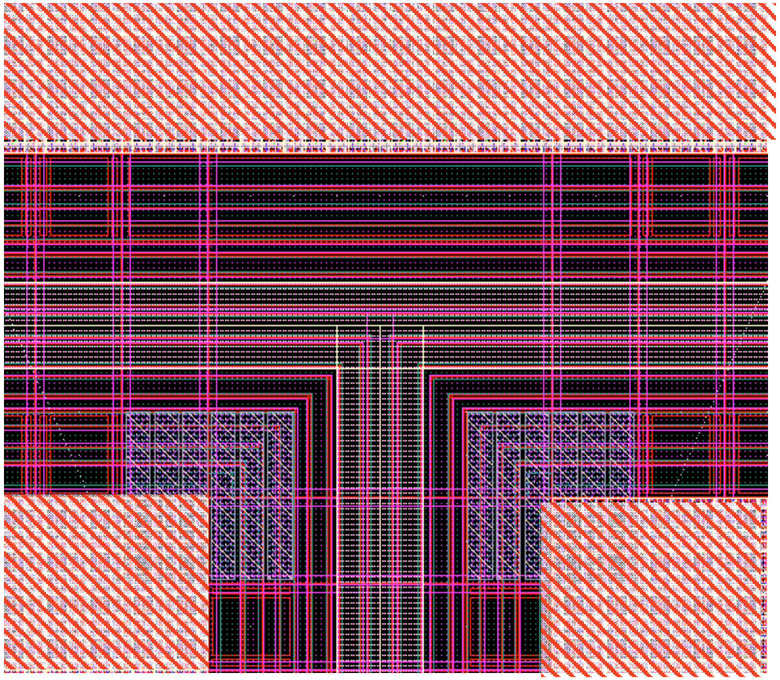
with 200μm shunt TL

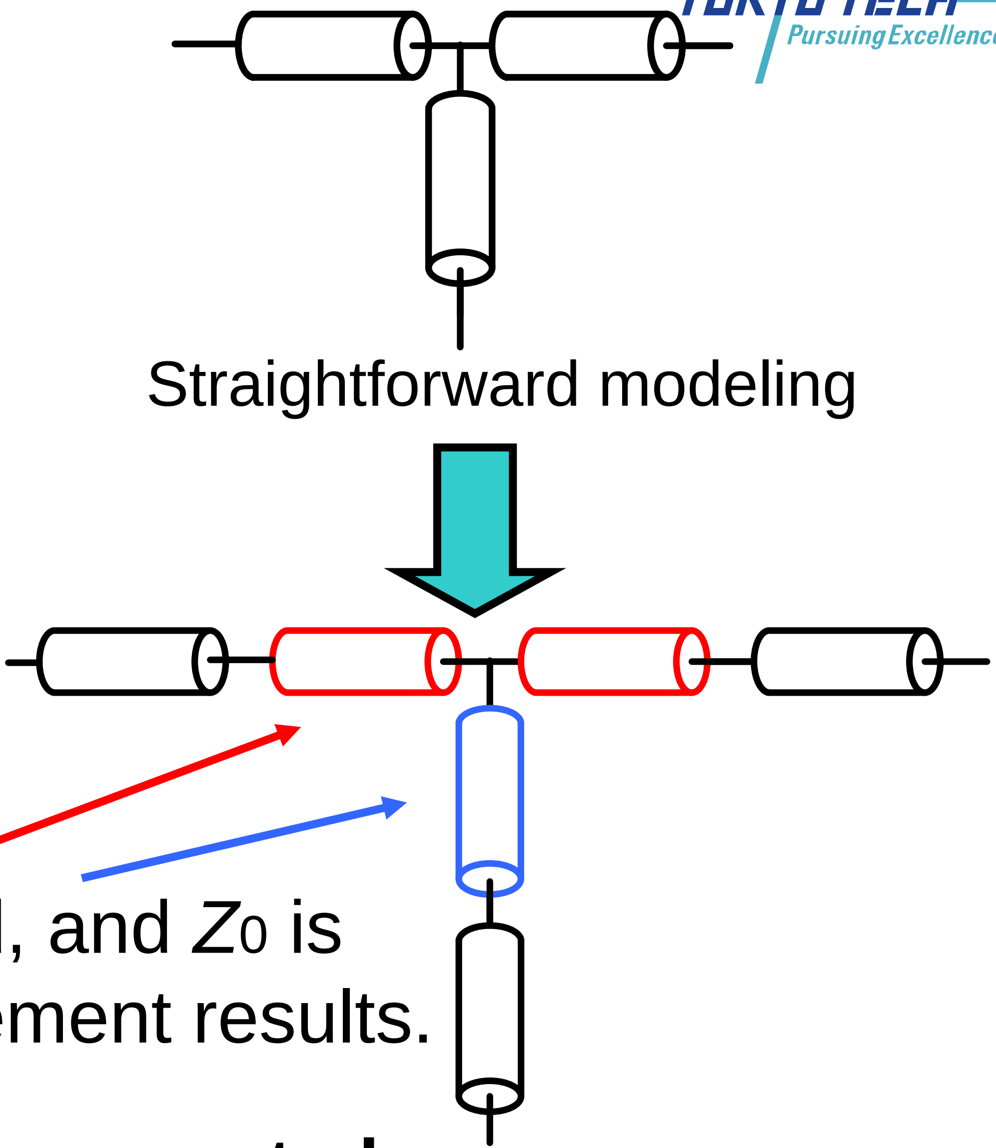


with 4 bending parts

Each red-box part is characterized as a combination of optimized transmission lines.

T-junction modeling

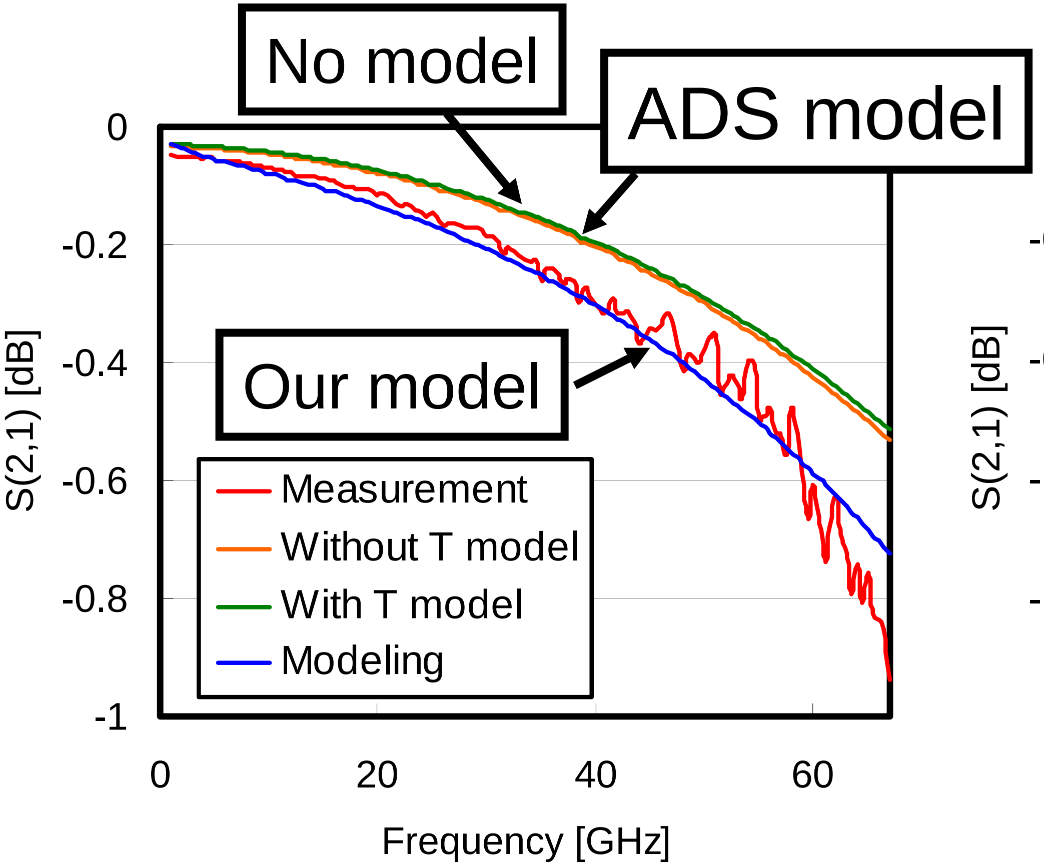




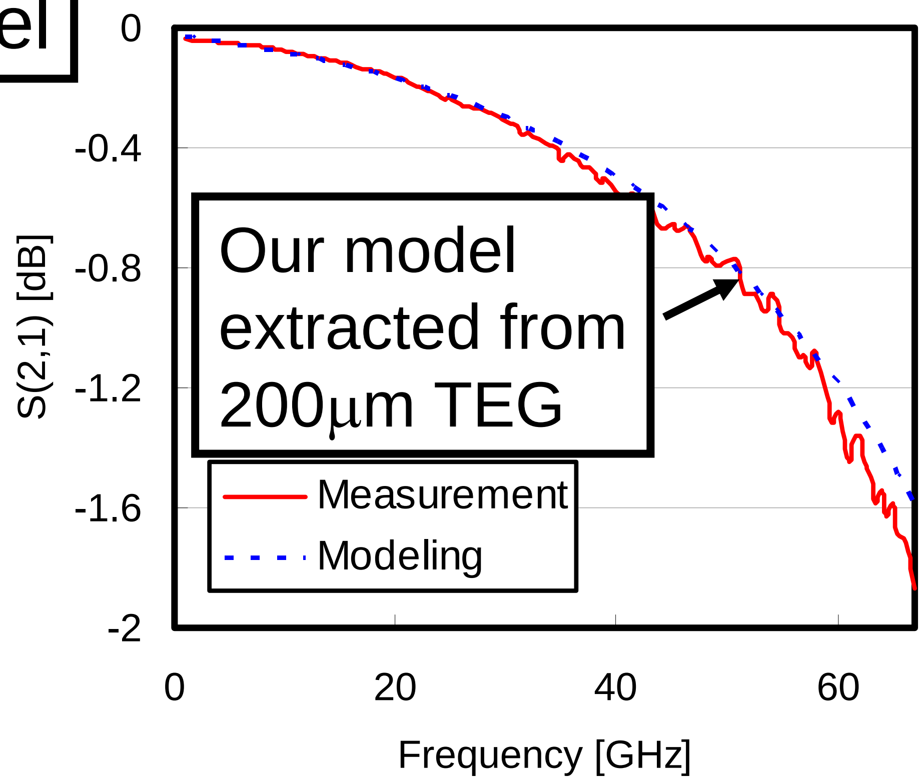
Lower Z_0 TLs are utilized, and Z_0 is adjusted for the measurement results.

Dummy metal causes unexpected response.

Experimental results for T-junction



T-junction with 200μm shunt TL

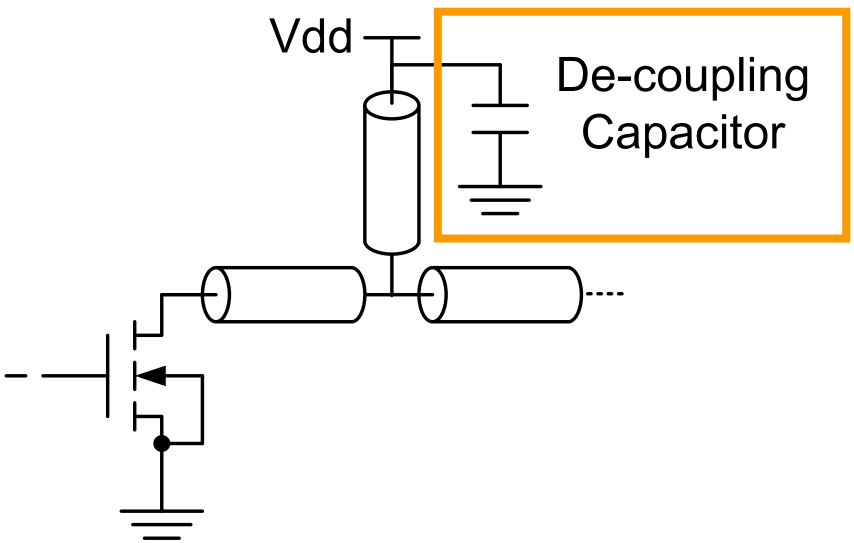


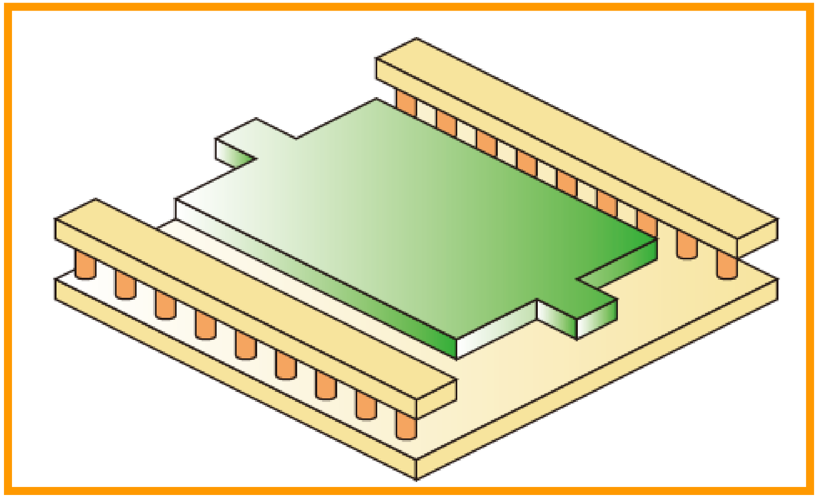
T-junction with 300μm shunt TL

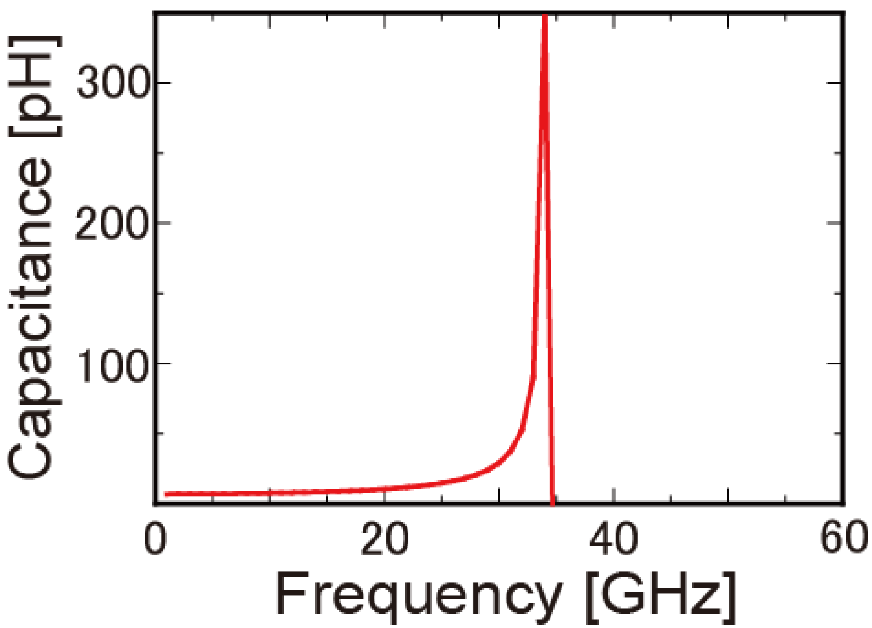
Overview of characterization

- Transmission line
- Branch & bend line
- Decoupling capacitor
- De-embedding patterns
- 1-stage amplifier
- DC probe
- 4-stage power amplifier

MIM capacitor for de-coupling



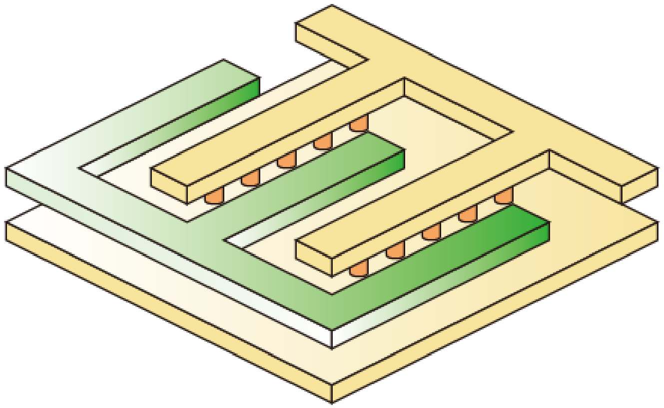




Area efficiency is large, but the self-resonance freq. is low.

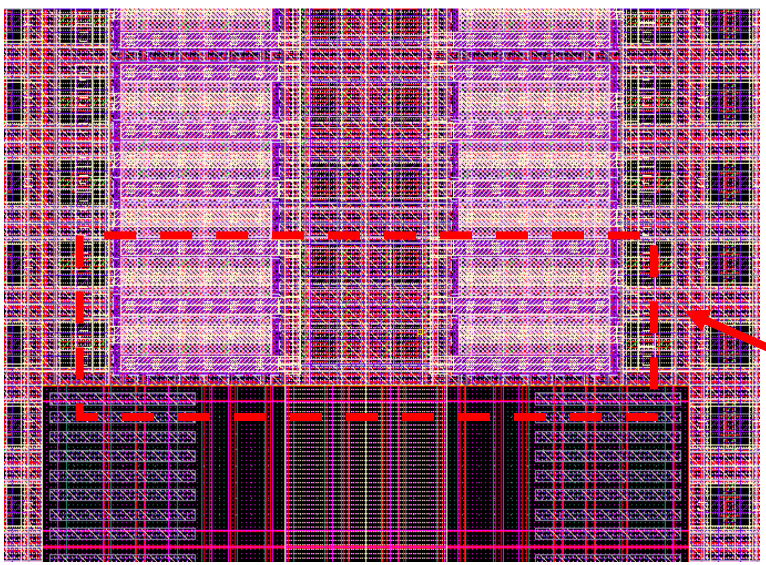
The regular layout of MIM cap. cannot be used at 60GHz.

Interdigital MIM capacitor



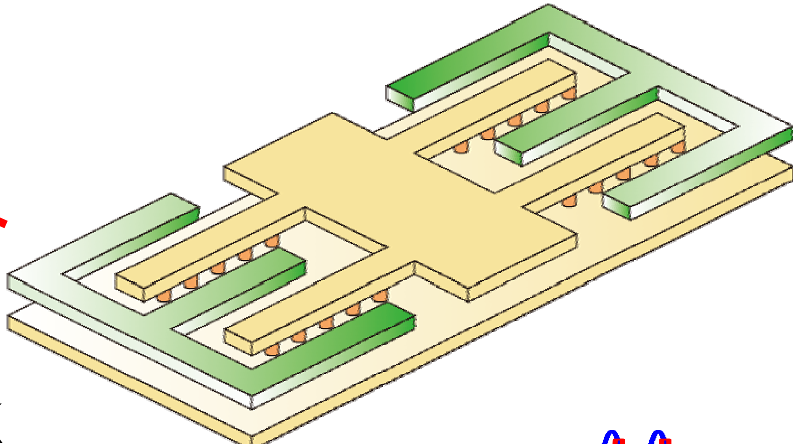
Interdigital structure with the optimized finger length is utilized.

↑ to DC-Pad



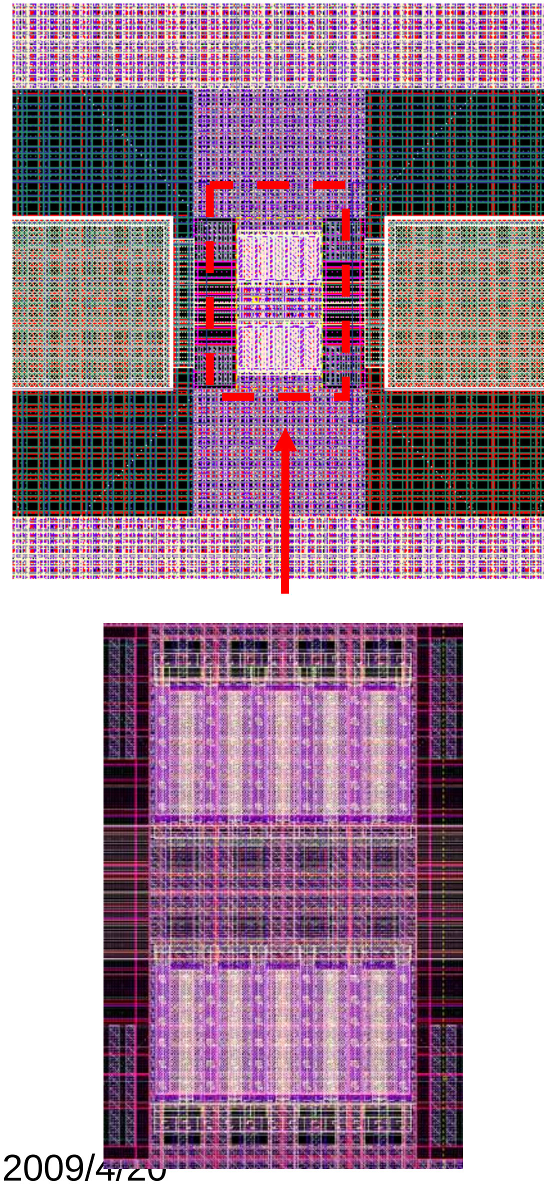
↓ to Matching block

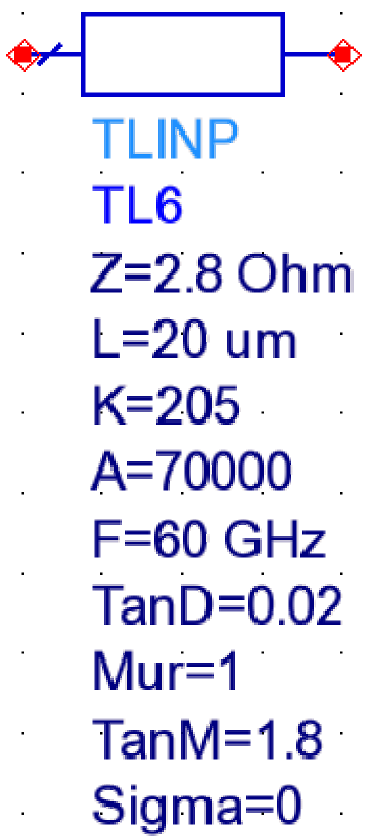
MIM cap. is modeled as a low-impedance transmission line.



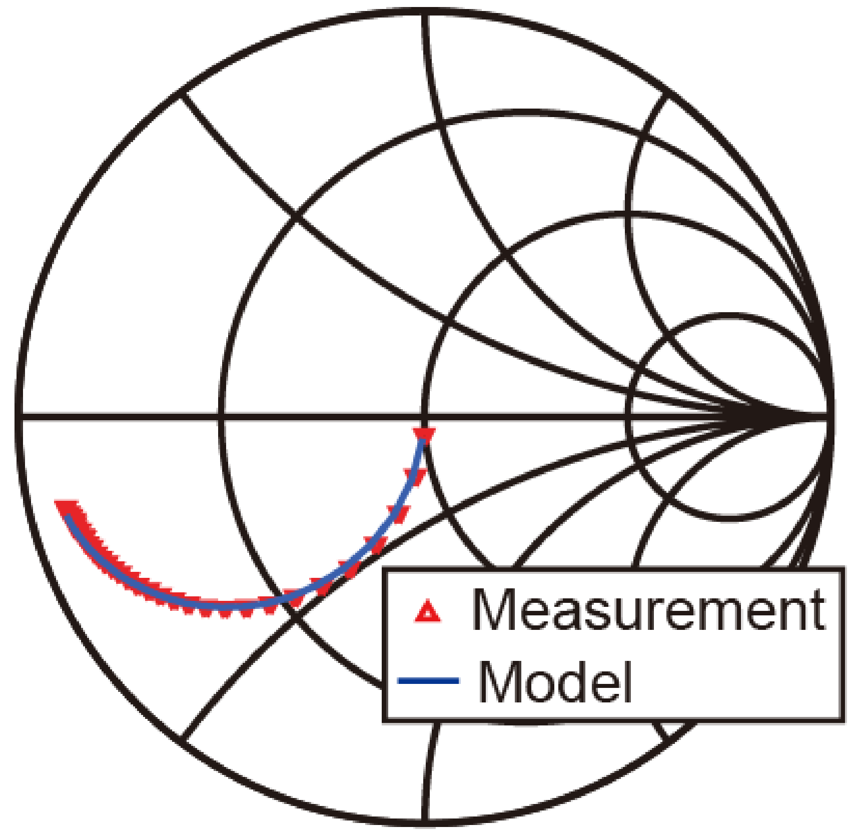
Distributed modeling of MIM cap.

Modeled as a transmission line





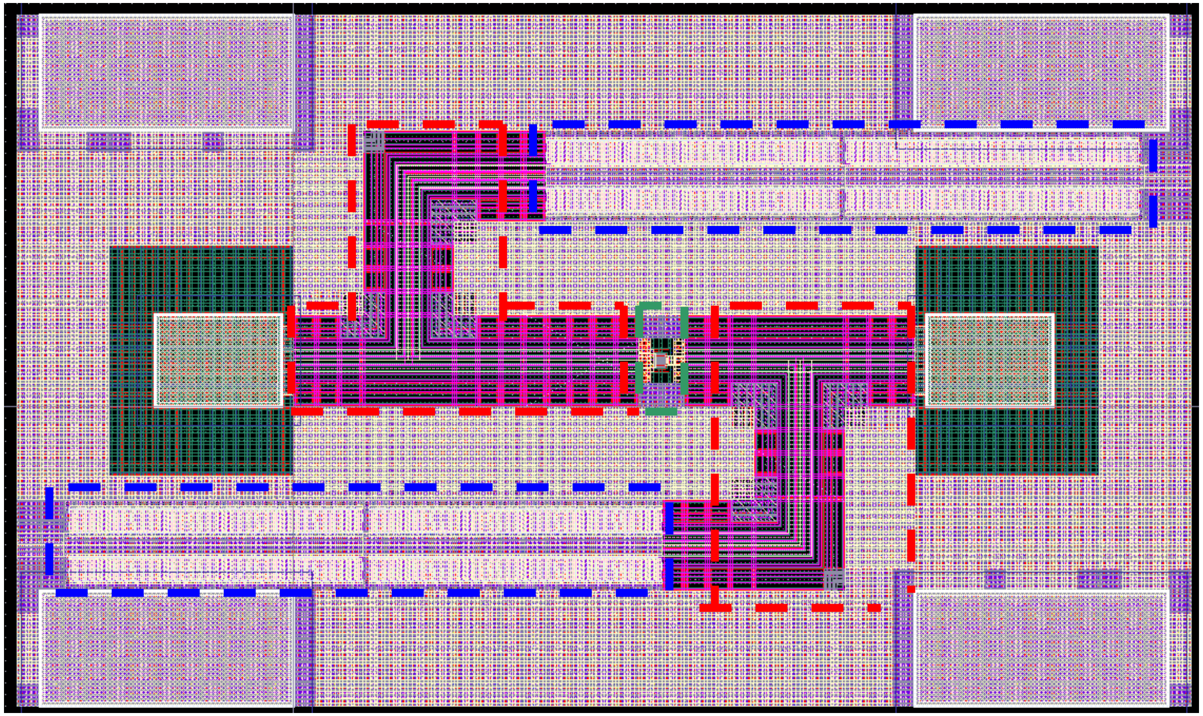
reflection 1-67GHz



Overview of characterization

- Transmission line
- Branch & bend line
- Decoupling capacitor
- De-embedding patterns
- 1-stage amplifier
- DC probe
- 4-stage power amplifier

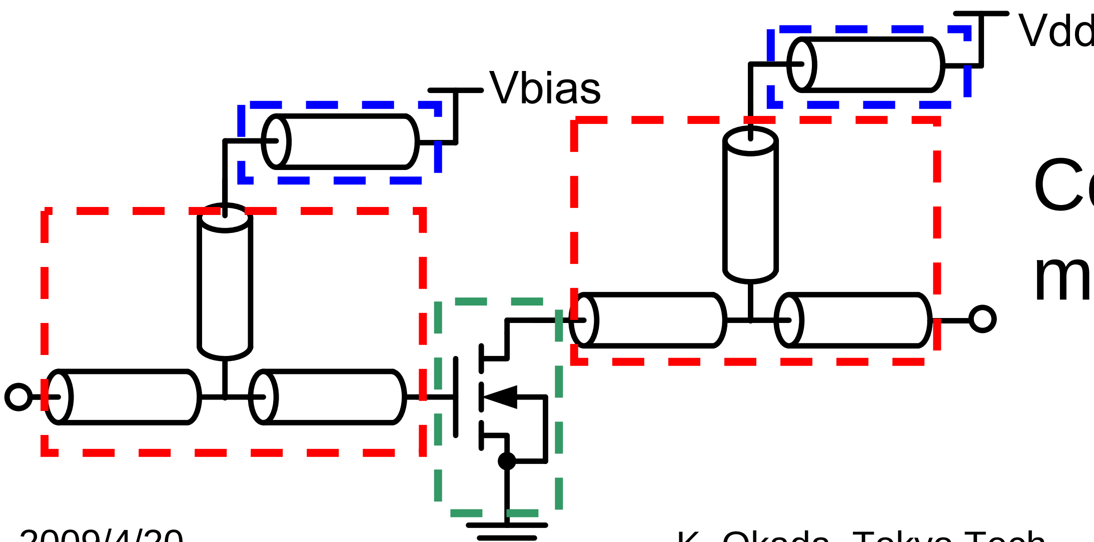
An evaluation using a 1-stage amplifier



: Transmission line

: De-coupling cap.

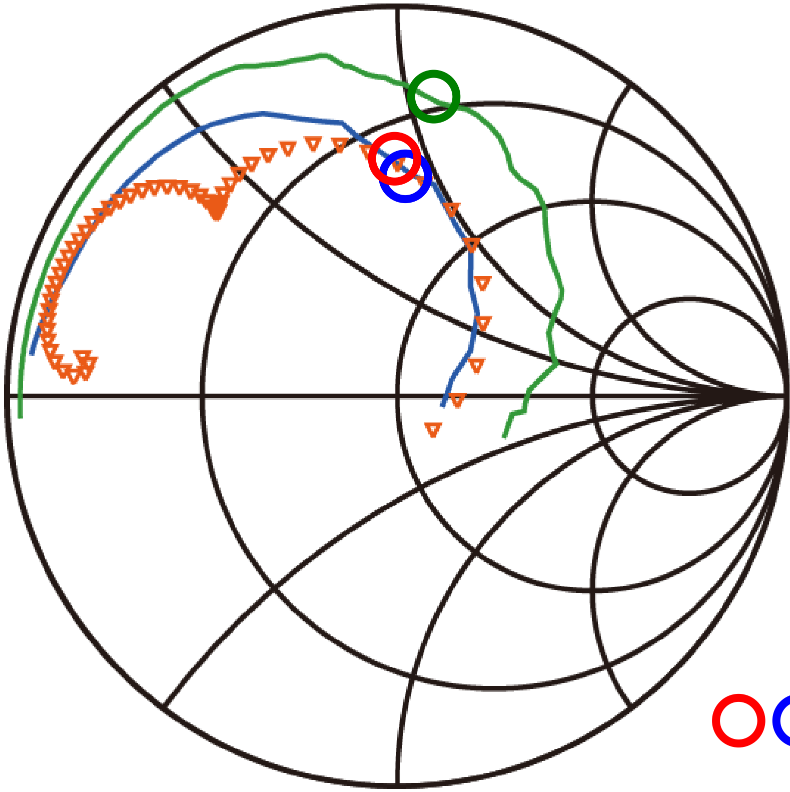
:CS Transistor (De-embedded S-parameter)



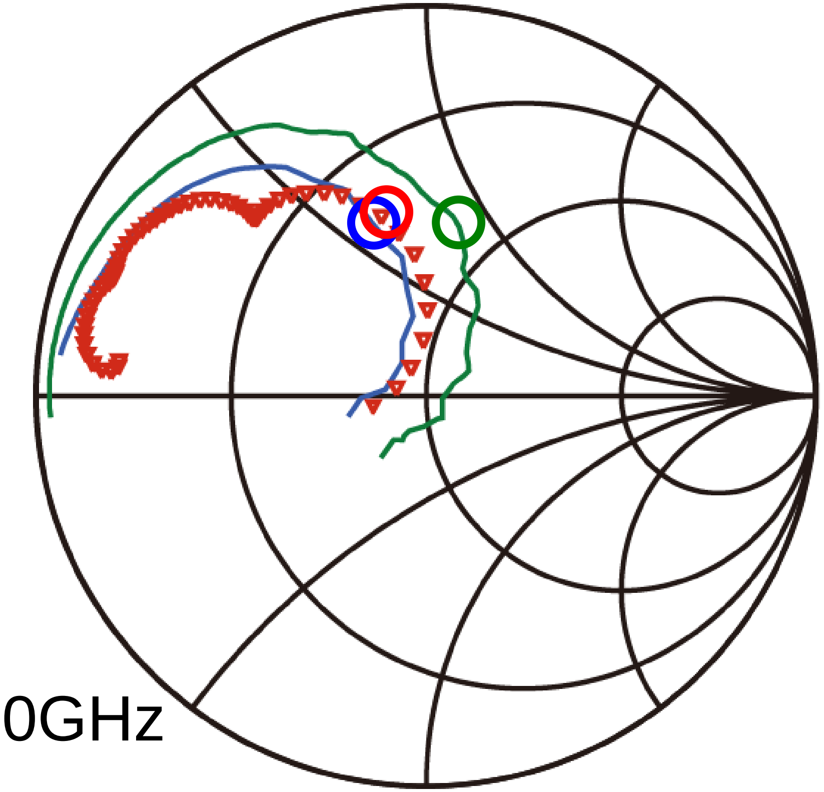
Comparison between model and measurement.

Model evaluation in input&output reflection

S_{11}(gate-side reflection)



S_{22}(drain-side reflection)



- Measurement
- with de-coupling model
- without de-coupling model

De-coupling MIM model is required for reliable design.

90nm CMOS is used.

Other modeling issues

- De-embedding
- Transistor layout optimization
- Spiral inductor
- Balun
- RF Pad
- DC probe / bonding wire / bump / filler / PCB

In-house PDK

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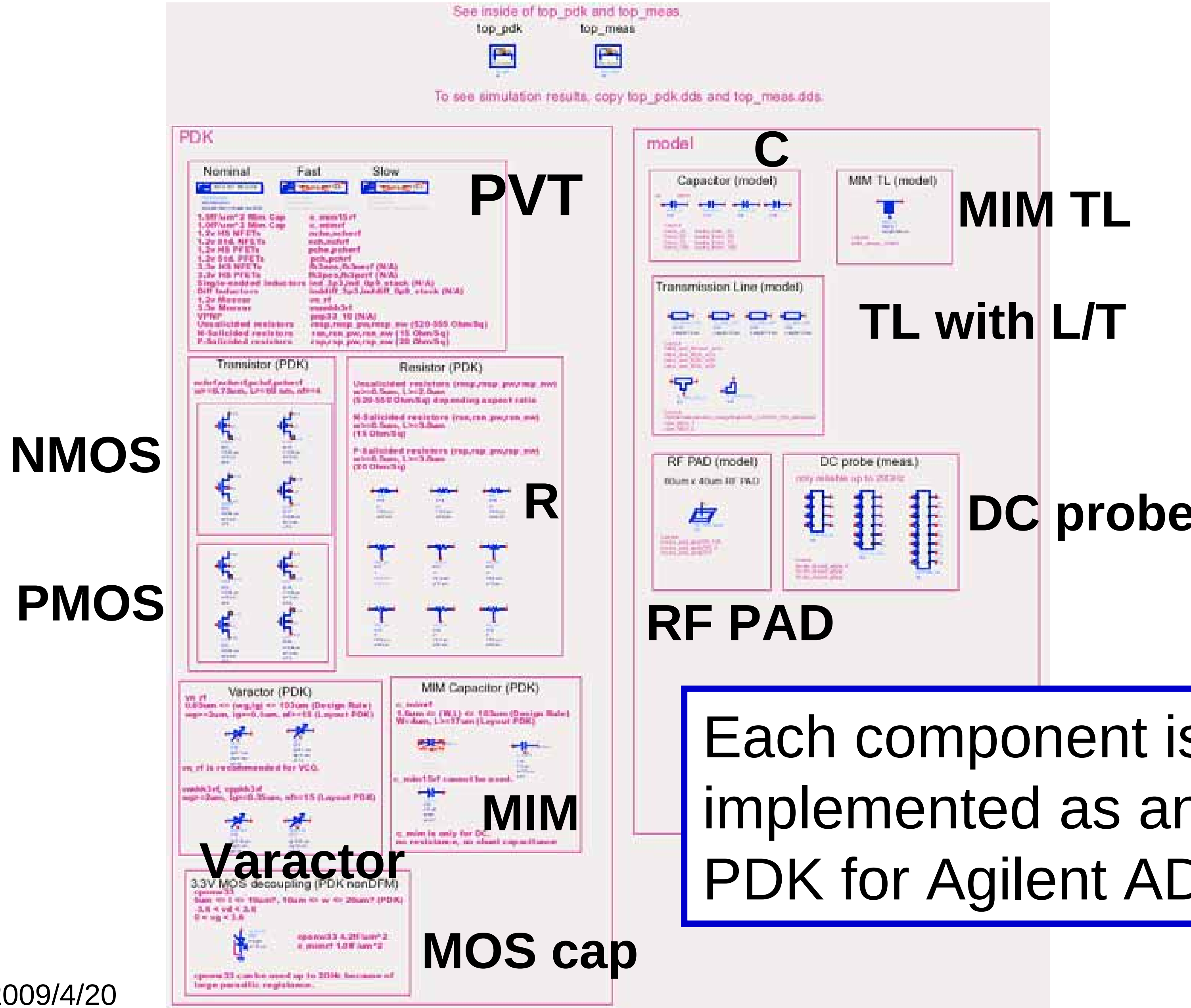


Each component is implemented as an in-house PDK for Agilent ADS.

Matsuzawa & Okada Lab.

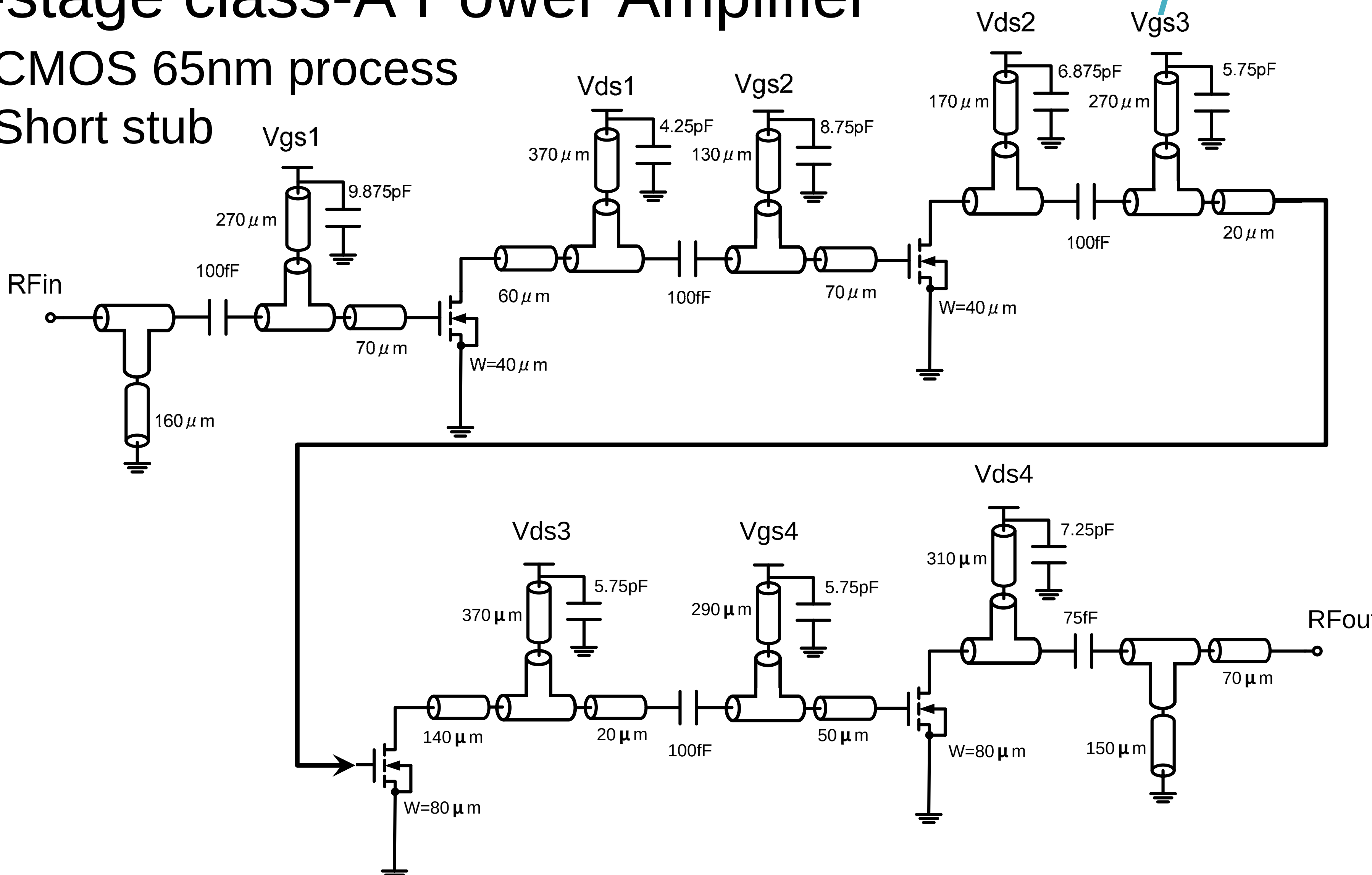
Overview of characterization

- Transmission line
- Branch & bend line
- Decoupling capacitor
- De-embedding patterns
- 1-stage amplifier
- DC probe
- 4-stage power amplifier

PA design

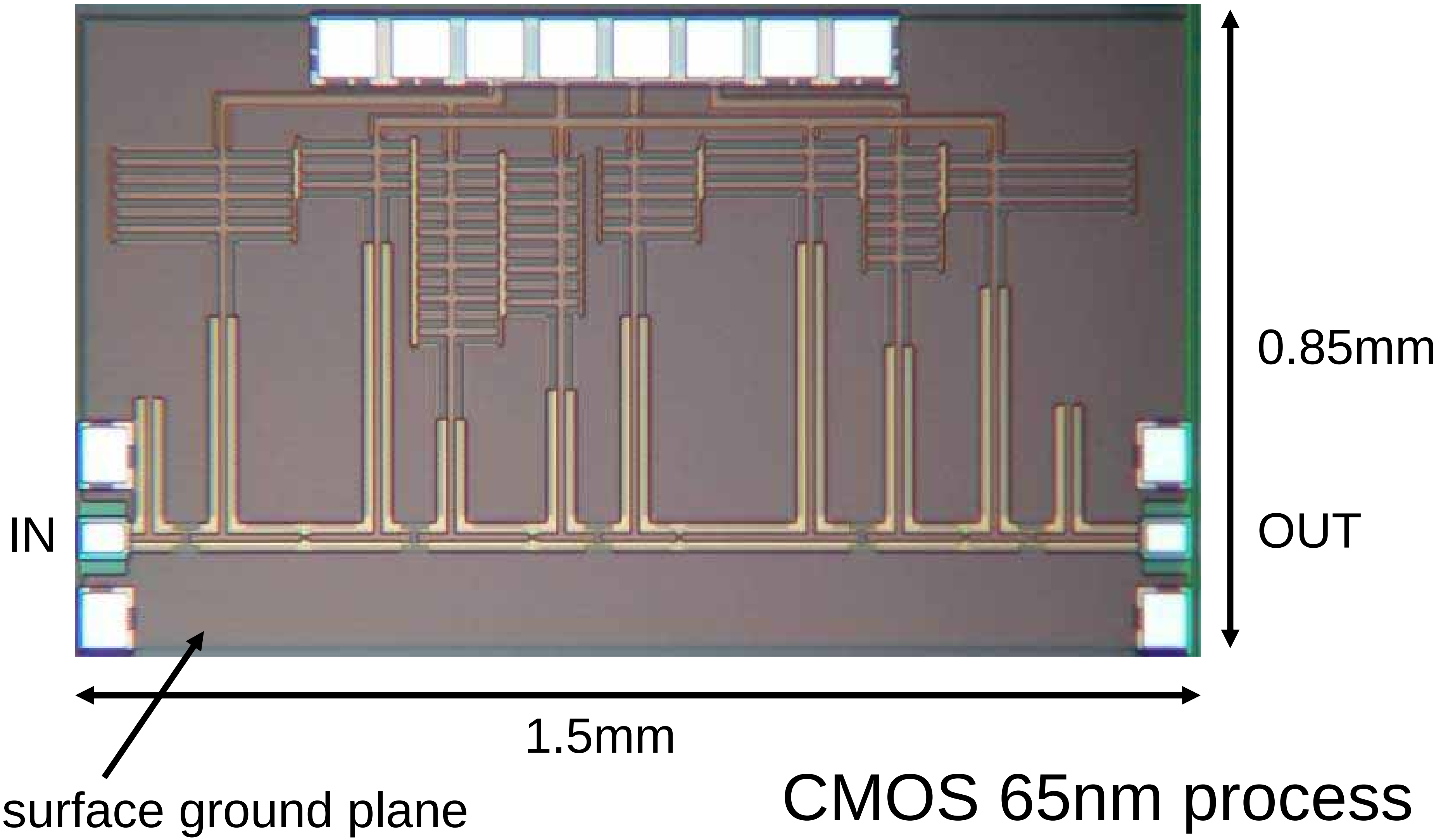
4-stage class-A Power Amplifier

- CMOS 65nm process
- Short stub



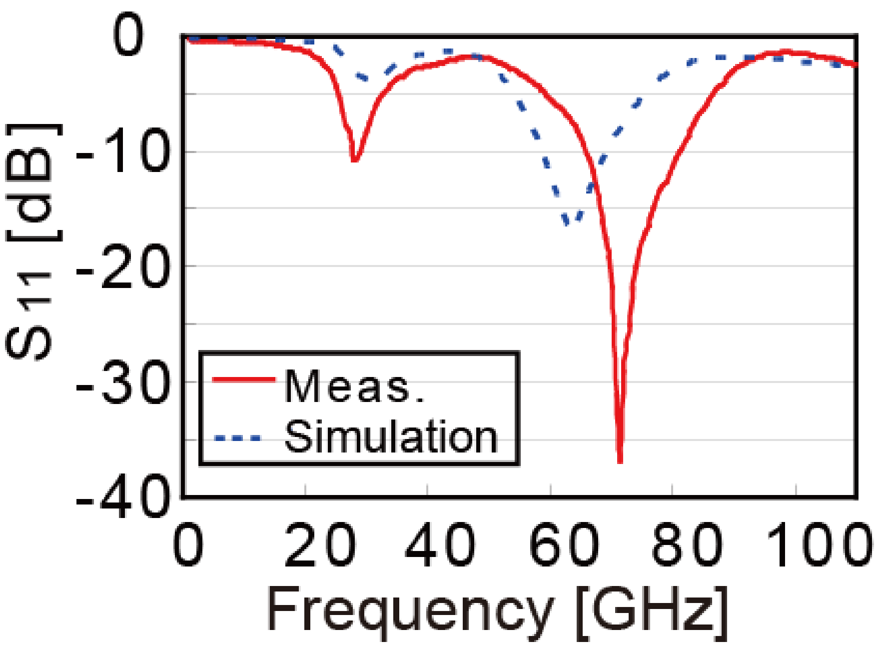
Chip micrograph

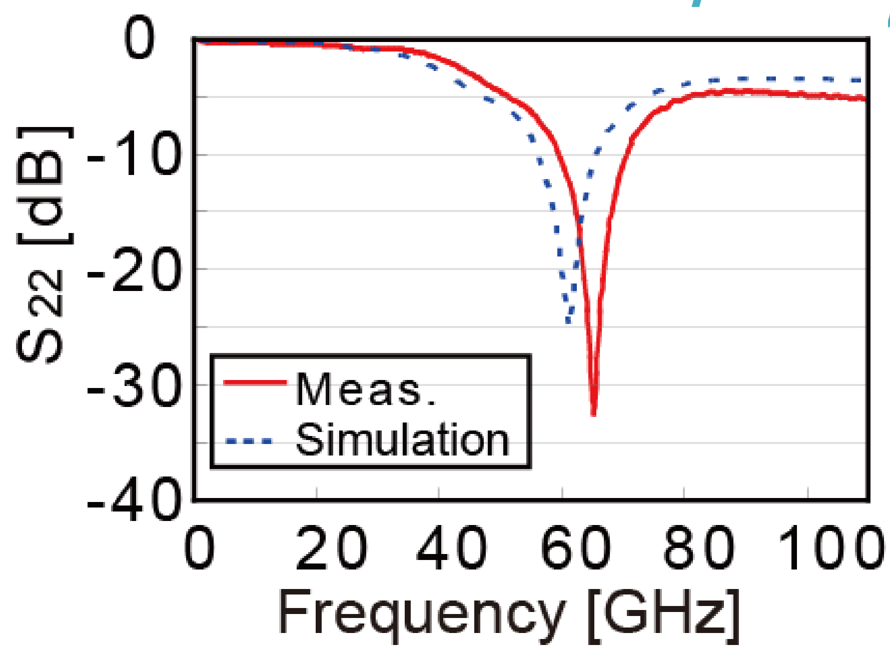
60GHz CMOS PA

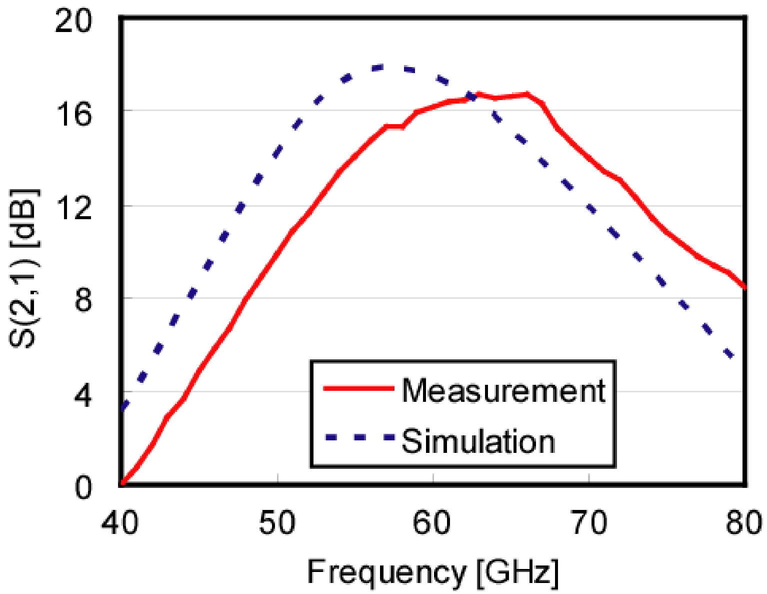


CMOS 65nm process

Measurement results







@61.5GHz

S_{21}: 16.4dB

S_{11}: <-8dB

S_{22}: <-10dB

Measurement results

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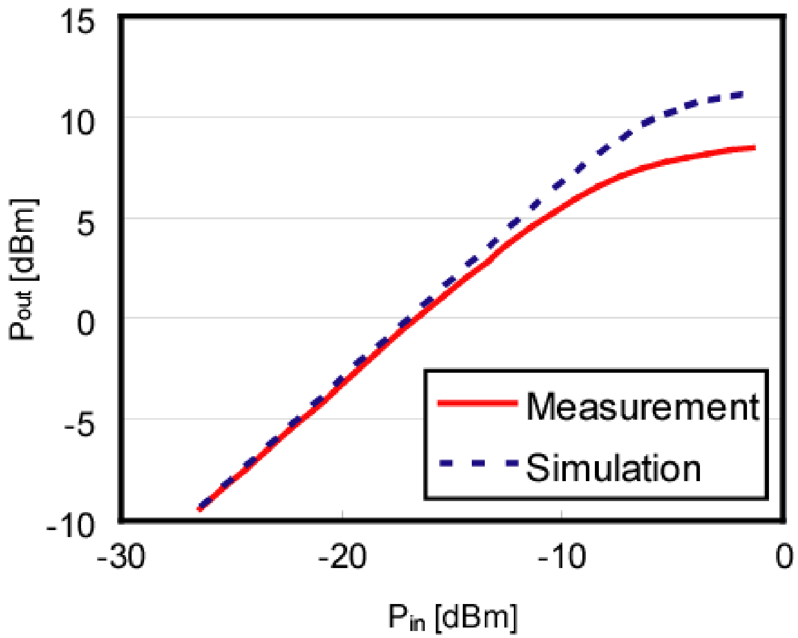

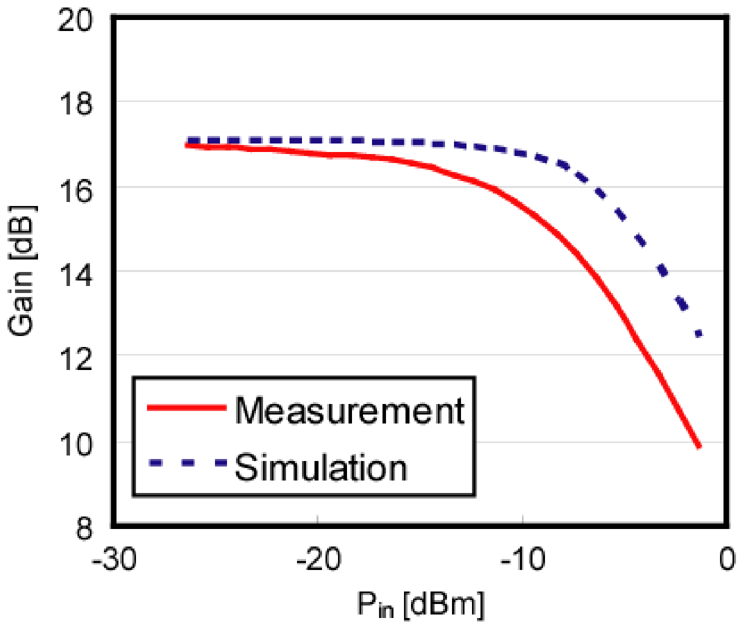

Power gain: 16.4dB

P_{1dB}: 4.6dBm

P_{DC}: 122mW

Measurement summary

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Reference	Technology	Freq. [GHz]	Gain [dB]	P_{1dB} [dBm]	PAE@P_{1dB} [%]	P_{DC} [mW]	V_{DD} [V]
[4] JSSCC 2007	90nm CMOS	61	5.2	6.4	7.4	21	1.5
[5] RFIC 2008	90nm CMOS	63	14	11	15	81	1.2
[6] ISSCC 2008	90nm CMOS	60	8.2	8.2	2.4	229	1.2
[7] ISSCC 2008	90nm CMOS	60	5.5	9	6	80	1
[8] ISSCC 2008	90nm CMOS	60	13.3	10.5	8	150	1
[9] ISSCC 2009	65nm CMOS	60	15.8	2.5	3.95	43.5	1
[10] ISSCC 2009	45nm CMOS	60	13.8	11	-	-	1.1
[11] MWCL 2009	90nm CMOS	60	30	10.3	6	178	1.8
This work	**65nm CMOS**	**61.5**	**16.4**	**4.6**	**2.3**	**122**	**1.2**

[4] T.Yao, *et al*., JSSC 2007(Tronto Univ.) [5] T.L.Rocca, *et al*., RFIC 2008 (UCLA) [6] T.Suzuki, *et al*., ISSCC 2008 (Fujitsu)
[7] D. Chowdhury, *et al*., ISSCC 2008 (UCB) [8] M. Tanomura, *et al*., ISSCC 2008 (NEC)
[9] W.L. Chan, *et al*., ISSCC 2009 (Delft Univ.) [10] K. Raczkowski, *et al*., ISSCC 2009 (KU Leuven&IMEC)
[11] J.-L.Kuo, *et al*., MWCL 2009 (NTU)

Summary & Conclusion

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In this presentation, I presented a modeling approach to design a 60GHz CMOS amplifiers.

1. Design issue of TL on CMOS chips is different from that of compound semiconductors.
   e.g., dummy metal, lossy substrate, large conductive loss, etc
2. Branch modeling
3. Distributed modeling of de-couple MIM cap.
4. Evaluation using a 1-stage amplifier

By the proposed modeling method, 60GHz power amplifier can be successfully realized.

Acknowledgement

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