アナログ・RF回路の先端設計技術動向

その2

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Contents

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Why CMOS?

- **Low cost**
  - **Must be biggest motivation**
  - **CMOS is 30-40% lower than Bi-CMOS**

- **High level system integration**
  - **CMOS is one or two generation advanced**
  - **CMOS can realize full system integration**

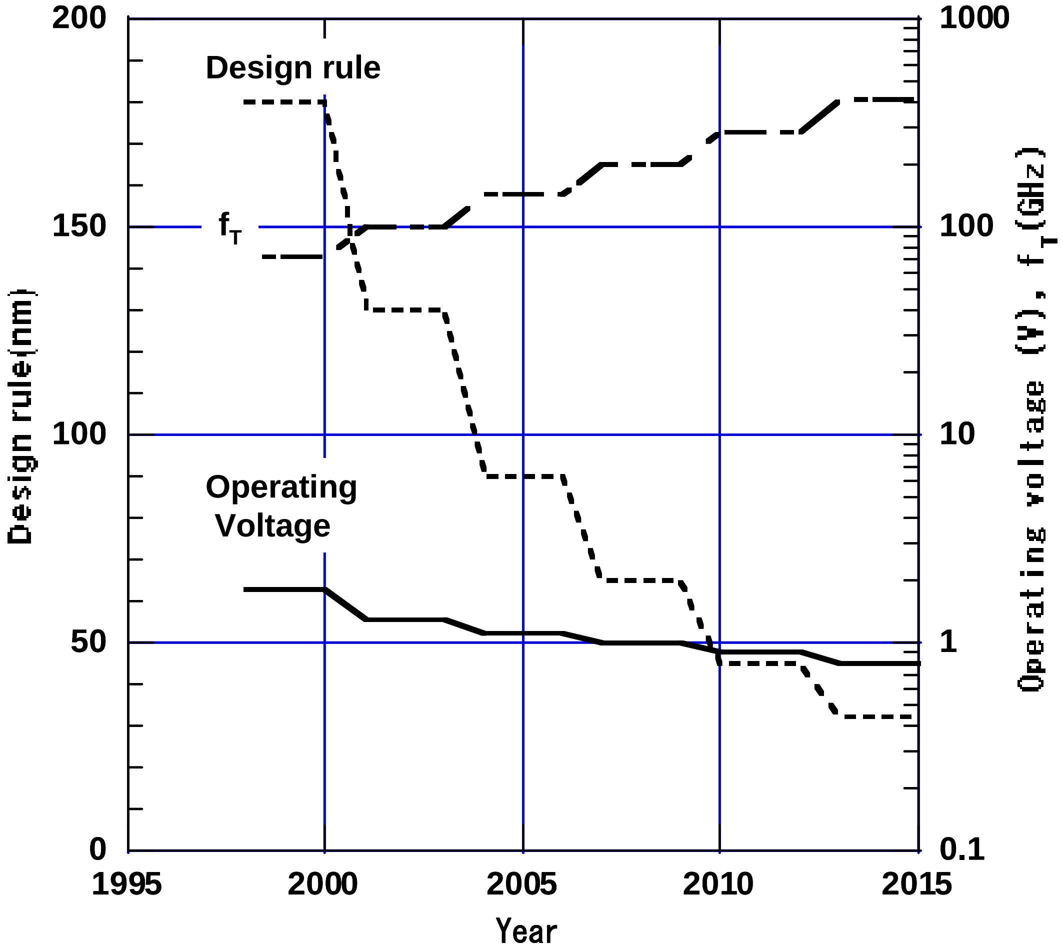
- **Stable supplyment and multi-foundries**
  - **Fabs for SiGe-BiCMOS are very limited.**
    → Slow price decrease and limited product capability

- **Easy to use**
  - **Universities and start-up companies can use CMOS with low usage fee, but SiGe is difficult to use such programs.**

f_T and operating voltage of CMOS

f_T is higher than 200GHz at 90nm NMOS and enables mm-wave application.

Operating voltage will be around 1V.



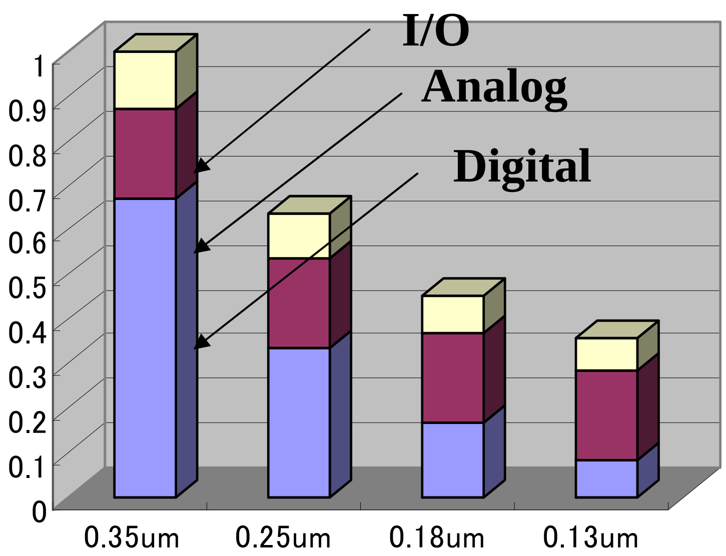
$$f_T \approx \frac{\upsilon_s}{2\pi L}$$

v_s: Saturation career velocity
L: Channel length

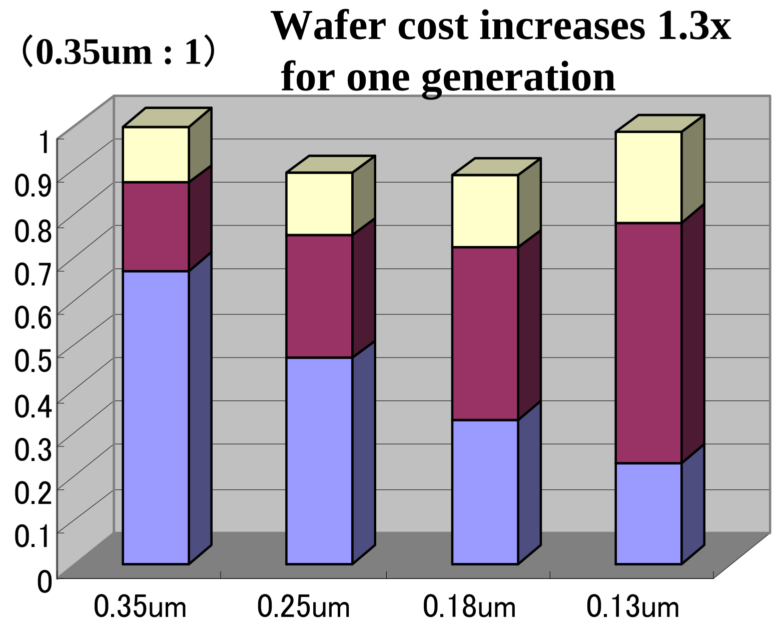
Cost up issue by analog parts

Cost of mixed A/D LSI will increase when using deep sub-micron device, due to the increase of cost of non-scalable analog parts.

Large analog may be unacceptable.
Some analog circuits should be replaced by digital circuits



Chip area



Chip cost

Akira Matsuzawa, "RF-SoC- Expectations and Required Conditions,"
IEEE Tran. On Microwave Theory and Techniques, Vol. 50, No. 1, pp. 245-253, Jan. 2002

Technology trend in RF CMOS LSI

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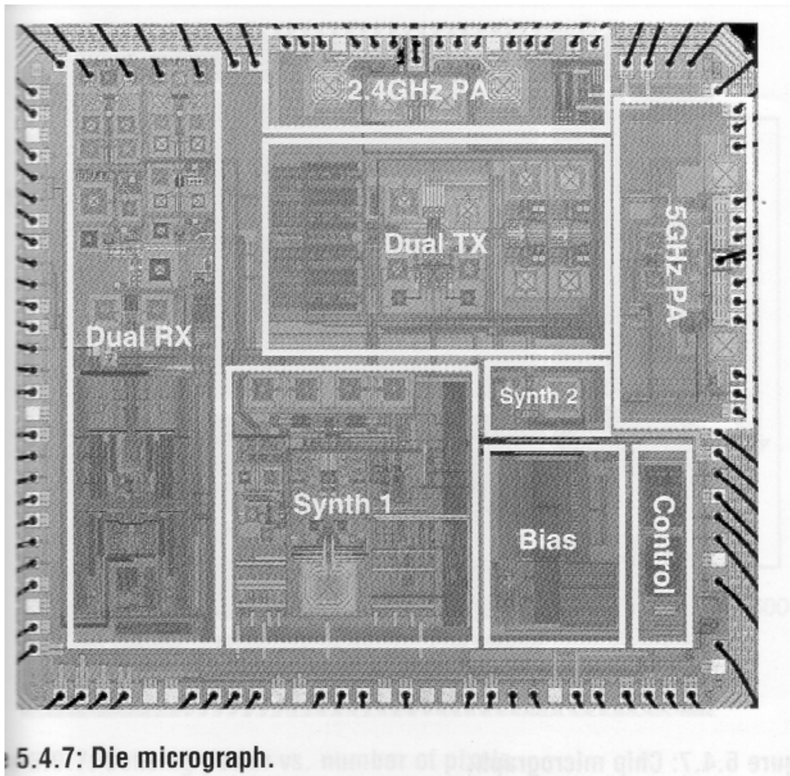
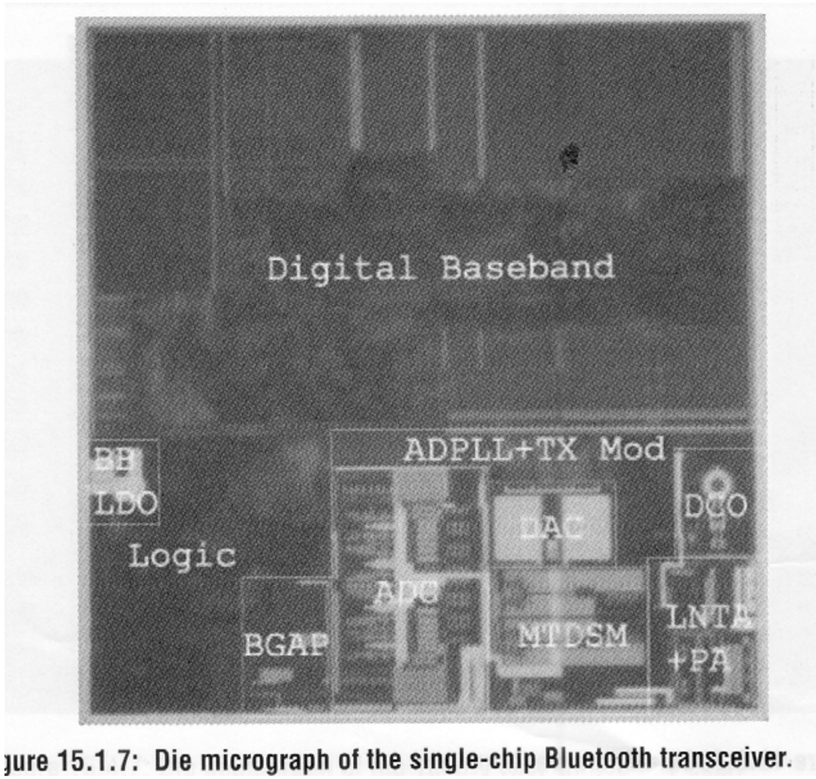
Analog centric RF CMOS will be replaced by digital centric RF CMOS.

Wireless LAN, 802.11 a/b/g
0.25um, 2.5V, 23mm^2, 5GHz



M. Zargari (Atheros), et al., ISSCC 2004, pp.96

Discrete-time Bluetooth
0.13um, 1.5V, 2.4GHz



K. Muhammad (TI), et al., ISSCC2004, pp.268

Technology trend in RF-CMOS LSI

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Analog-centric RF CMOS will be replaced by digital-centric RF CMOS.
High performance, low cost, stable and robust circuits,
no or less external components, no adjustment points,
and high testability are the keys. DSP and ADC will play important role.

Analog-centric → **Digital-centric**

	Analog-centric	Digital-centric
Signal processing	**Analog circuits** **Analog processing** **+External component**	**DSP+ADC** **+ Small and robust analog ckts.**
Adjustment	**External**	**Digital on chip, no external**
External components	**Large #**	**No or less**

RF-CMOS SoC for FM/AM tuner

Courtesy Niigata-Seimitsu Co., Ltd.

Current AM/ FM tuner system

Current AM/FM tuner uses 3 ICs and large # of external components. Furthermore 12 adjustment points are needed.

Large # of products, but not expensive product. More efforts for the cost reduction are still needed.

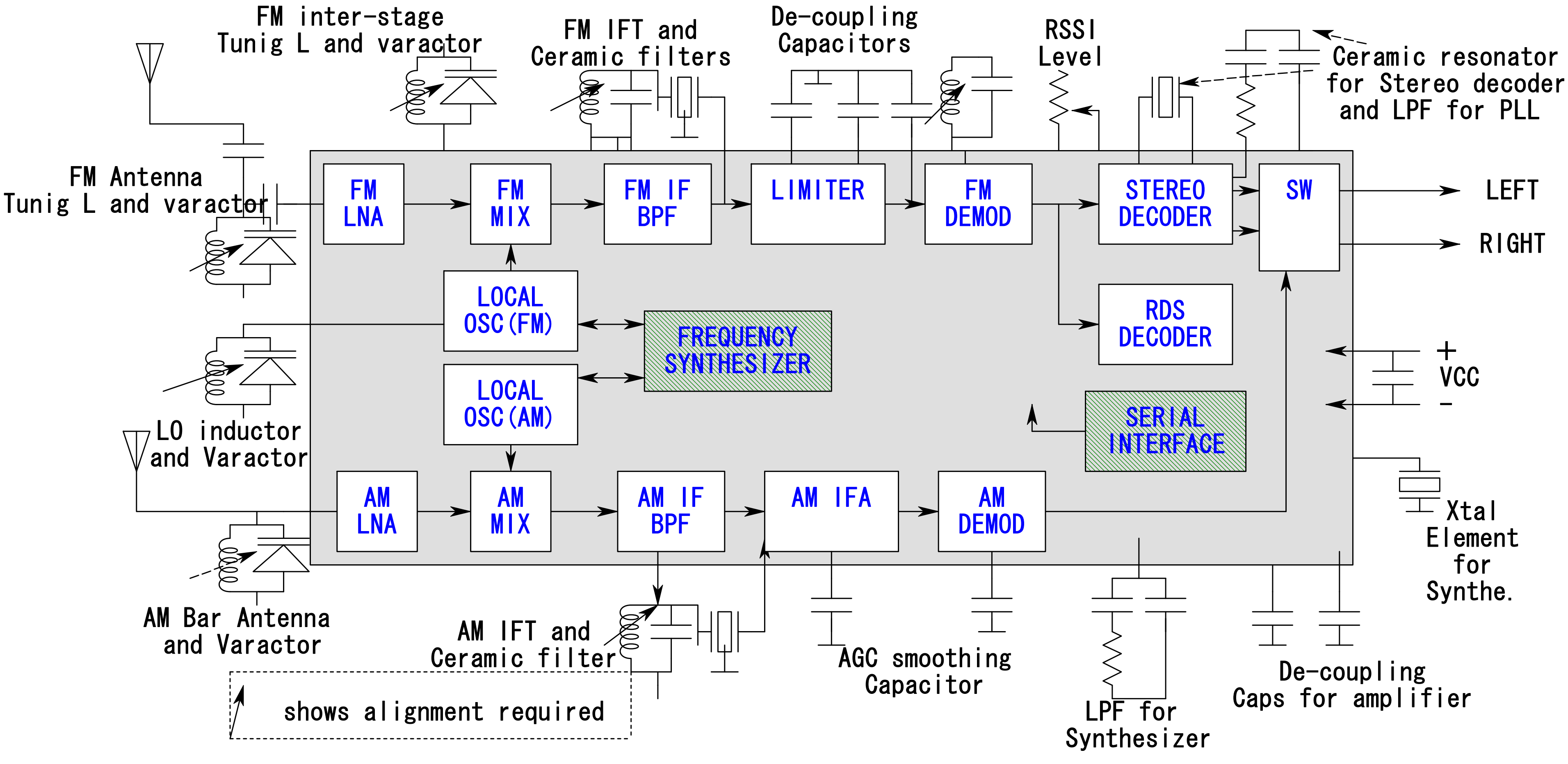
Bipolar IC = 1 (RF)
CMOS IC = 2 (PLL, RDS)
External Components=187

AM/FM Tuner for home use

12 adjustment points

Block diagram of current FM/AM tuner

Large # of external components. They should be integrated on a chip.



External parts used in existing IC

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Large # of external components are needed to analog signal processing.

External Parts	Blocks to be used
System	FM: Single conversion super heterodyne. IF=10.7MHz AM: Single or Double conversion super heterodyne IF=450KHz or 10.7MHz + 450KHz
Resistor	AGC, bias, LPF for PLL
Semi-fixed and Variable resistor	RSSI level alignment, volume control
Ceramic capacitor Small value capacitor	RF bypass, coupling, de-coupling
Electrolytic capacitor	AGC smoother, power-ground decoupling
Inductor	RF tuning, local oscillator, IF transformer, FM detector
Variable capacitance	RF tuning, Local oscillator
Analog filter	Noise canceller, LPF
Ceramic filter	FM and AM IF BPF for channel filter
Xtal Osc. element	System clock, Reference for PLL synthesizer
Total number of external parts	Home tuner and radio cassette tuner : around 165pcs Car tuner : 80 to 130pcs

Issues and conventional solutions of AM/FM tuner

Application of CMOS technology to AM/FM tuner looks very difficult, due to lower frequency and high dynamic range.

Lower frequency

AM: 522 KHz to 1710 KHz
SW: 2.3MHz to 26MHz
FM: 87.5 to 108 MHz

Larger Inductance and capacitance → **External components**

Serious 1/f noise → **Bipolar**

High dynamic range

AM: 14 dBuV to 126 dBuV
FM: 0 dBuV to 126 dBuV

Sharp and fine filter → **External filters (Ceramic)**

External varactors

High linearity ckt. → **Bipolar**

1st trial by CMOS technology

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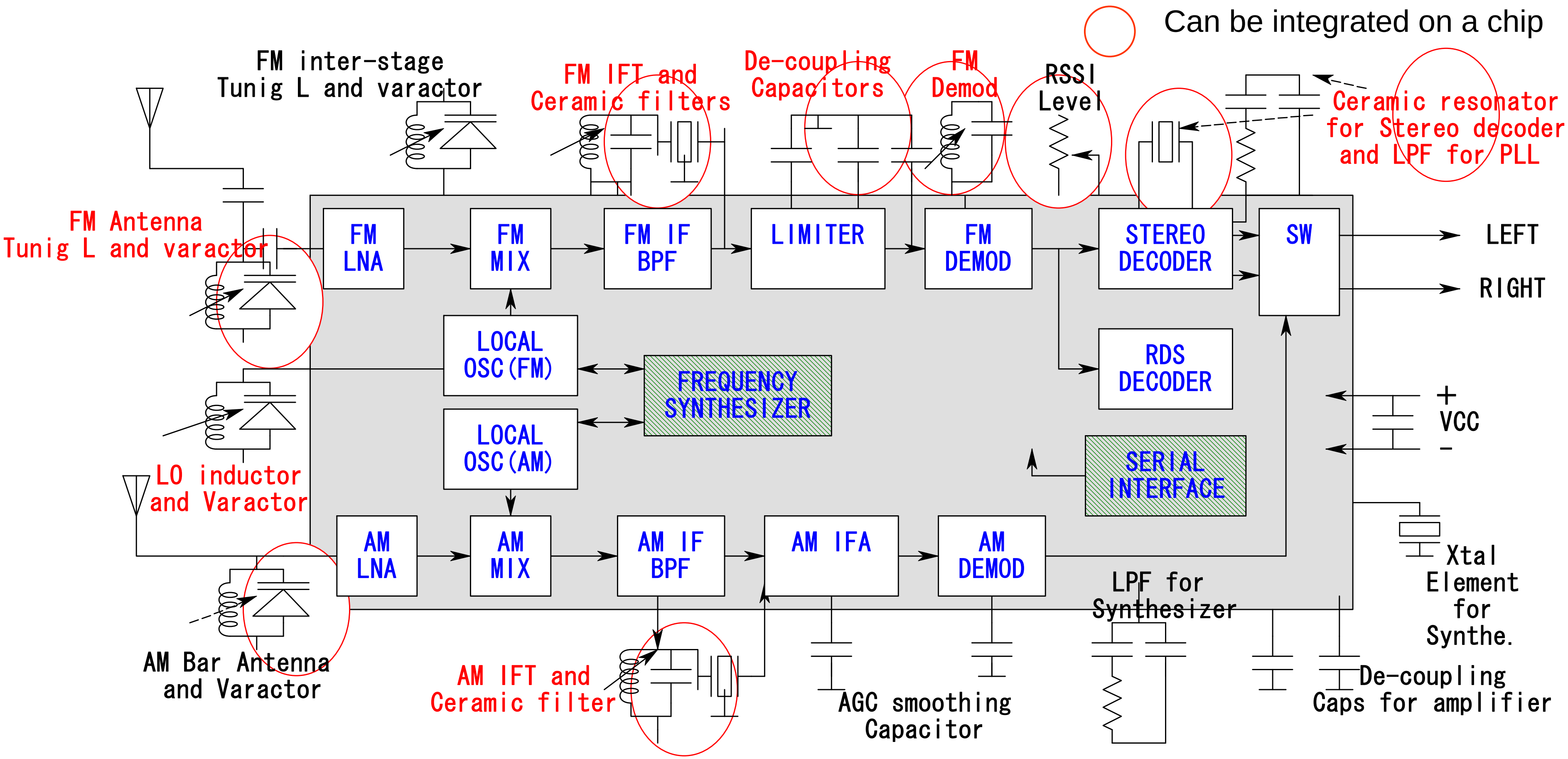
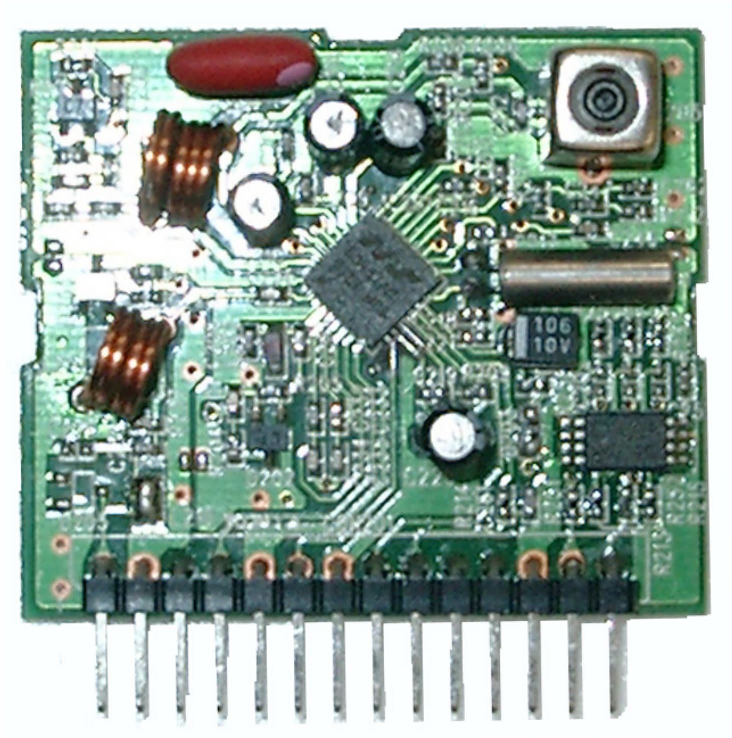
1st trial to realize AM/FM tuner by CMOS technology, many external components should be reduced.



Matsuzawa & Okada Lab.

Result of analog-centric CMOS tuner

Characteristics is affected by process variation easily.
Element mismatch causes DC offset, noise, distortion, and low filter performance.
The reduction of # of external components is not attractive for users.



External components 187→ 69

Analog-centric CMOS tuner technology

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1st trial was analog-centric CMOS tuner technology.

Circuits have been replaced by CMOS, however still use analog technology. Thus it had many issues and many external components were still needed.

Parts	Methods for on-chip	Problems
AM/FM IF BPF	1. Low IF(a few hundred KHz) 2.Gm-C BPF with auto alignment, SCF	1.poor selectivity(-45dB), 2. SCF Switch noise 3. Center frequency shift by DC offset 4. Poor image rejection ratio (25 to 35dB)
FM Demodulator	Pulse count FM detector	Poor THD (0.5%)
Stereo Decoder	Multi-vibrator VCO, SCF filter	Large variation of free-run frequency Still need external LPF for PLL
RSSI Level adj.	Signal detector with DC compensation	Can't cover all process corner
Varactor	MOS varactor	Too much sharp C-V curve, distorted signal
AGC smoother	Time division charge and discharge	Needs large capacitor for low audio frequency
Capacitors	Stages Direct connection, use small value coupling capacitor	High impedance required, Difficult for low frequency

Issues and advanced solutions of AM/FM tuner

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Lower frequency

AM: 522 KHz to 1710 KHz
SW: 2.3MHz to 26MHz
FM: 87.5 to 108 MHz

Larger Inductance and capacitance → **Digital filter, Mixer, PLL**
GHz OSC with divider

Serious 1/f noise → **PMOS**

Larger signal dynamic range

AM: 14 dBuV to 126 dBuV
FM: 0 dBuV to 126 dBuV

Sharp and fine filter → **Digital Signal processing**
With high resolution ADC
IF Freq. changed from
10.7 MHz to several 100 KHz

High linearity ckt. → **High resolution ADC**
Switch mixer
Watching desired and undesired signals

Advanced CMOS tuner

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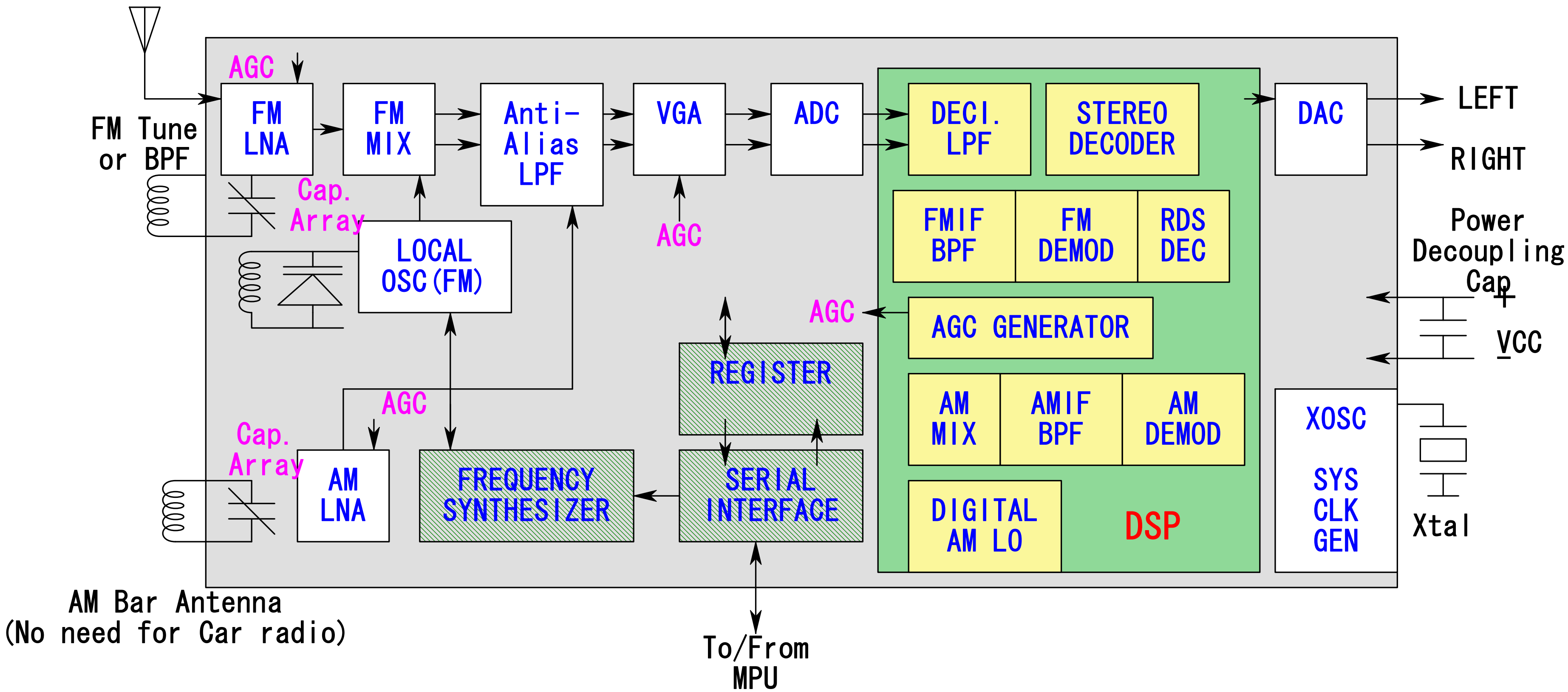
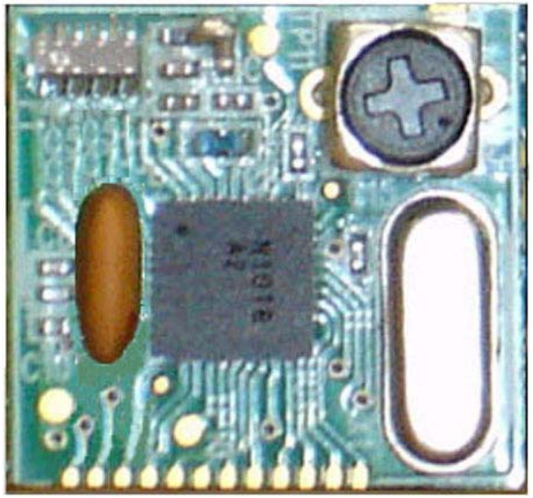
Digital-centric CMOS tuner has been developed.



Matsuzawa & Okada Lab.

Digital-centric CMOS tuner

One-chip CMOS tuner has been successfully developed.
It can attain high tuner performance and
can reduce the # of external components.
Furthermore it can realize no adjustment points.



Full CMOS one-chip solution

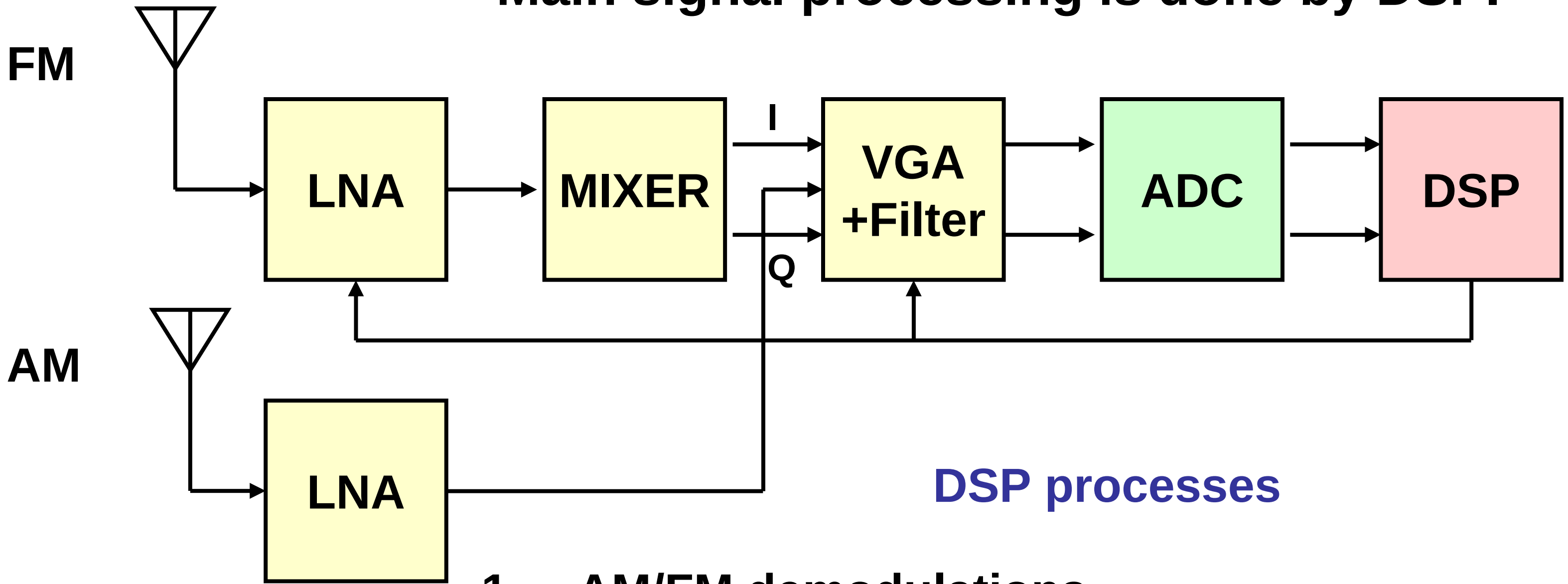
# of external components are 11

No adjustment points

Sensitivity: FM: 9dBuV, AM: 16dBuV
Selectivity: FM/AM >65dB
SNR: FM: 63dB, AM: 53dB
Stereo sep: 55dB
Image ratio: FM: 65dB, AM: Infinity
Distortion: FM: 0.09%, AM=0.25%

Digital-centric CMOS tuner technology

Main signal processing is done by DSP.



DSP processes

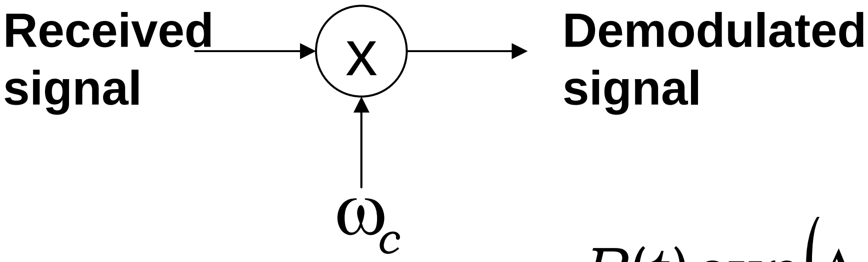
1. AM/FM demodulations
2. Stereo decoder
3. AM mixer
4. Channel select filter
5. Support for image reject
6. Watch the signal revel and control gain of each stage
7. Parameter control and adjustment with MCU

Demodulation of AM/FM signal

AM/ FM signals can be demodulated by simple arithmetic operations

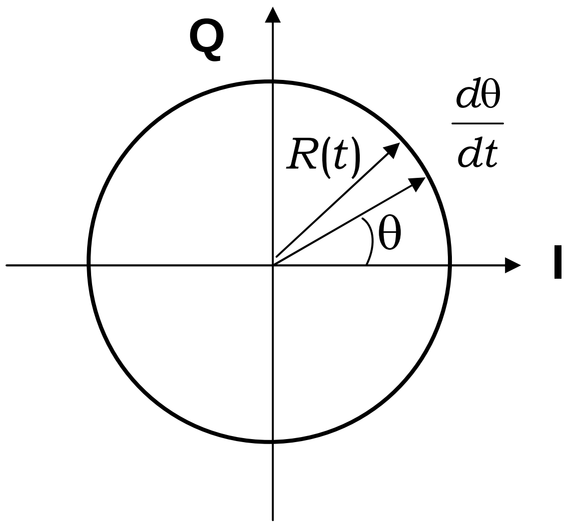
1) AM demodulation

$$[1+S(t)]\cdot \exp(j\omega_c t)\times \exp(-j\omega_c t) = 1 + S(t)$$



2) FM demodulation

$$R(t)\exp\left(\Delta j\omega t + jK_d\int m(\tau)d\tau\right)$$



$\Delta\omega$: *Frequency offset*

$R(t)$: *Amplitude variation*

$m(\tau)$: *Baseband signal to be recovered*

$$\theta = \Delta\omega t + K_d\int m(\tau)d\tau$$

$$\frac{d\theta}{dt} = \Delta\omega + K_d m(t)$$

m(t) can be demodulated

Stereo decoder

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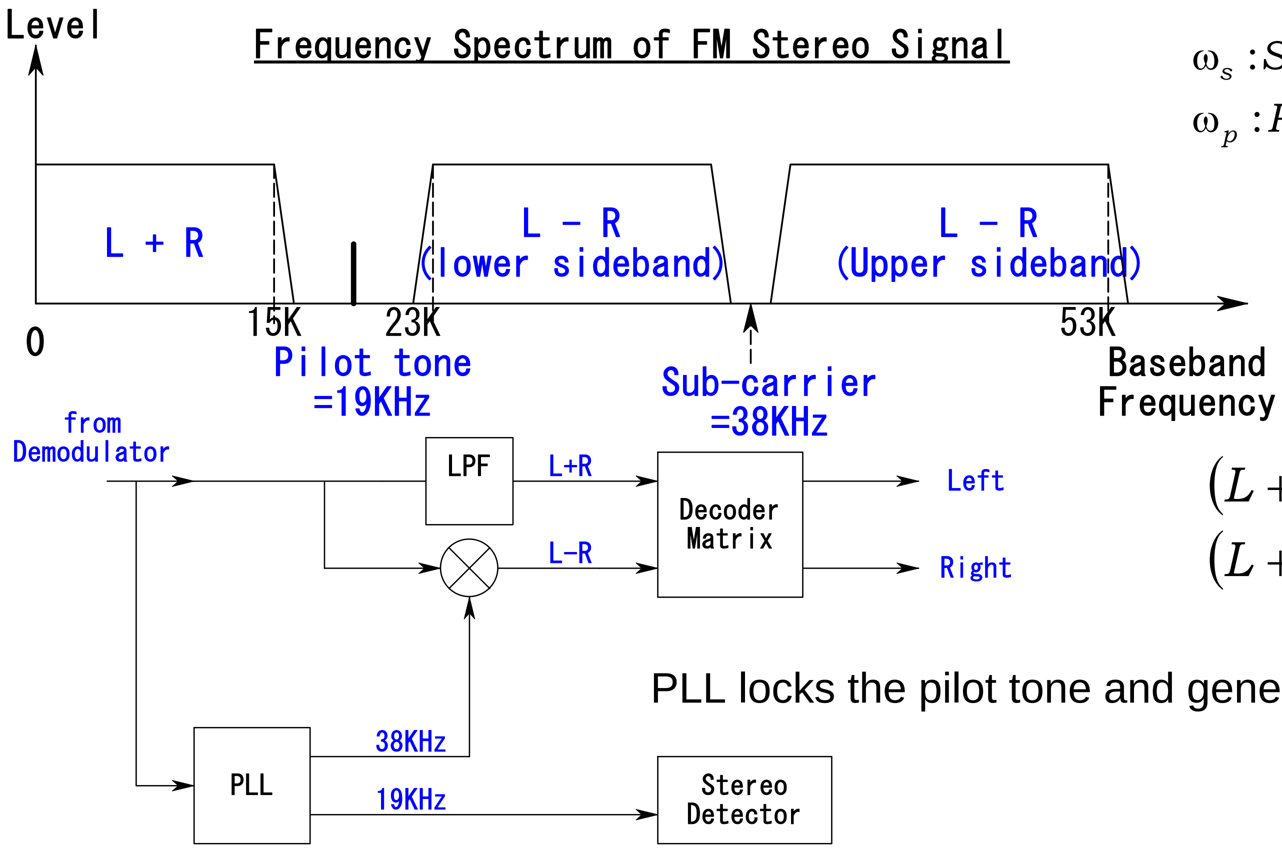
Te stereo signal can be reconstructed by numerical PLL, mixer, and filter.

$$S(t) = (L+R) + (L-R)\cos\omega_s t + K\cos\omega_p t$$



ω_s : $Sub-carrier = 38KHz$

ω_p : $Pilot\ tone = 19KHz$

$$(L+R)+(L-R) = 2L$$

$$(L+R)-(L-R) = 2R$$

PLL locks the pilot tone and generates 38KHz for sub-carrier

Image rejection in low IF receiver

Image signal can be rejected by using I/Q mixer and phase shift.

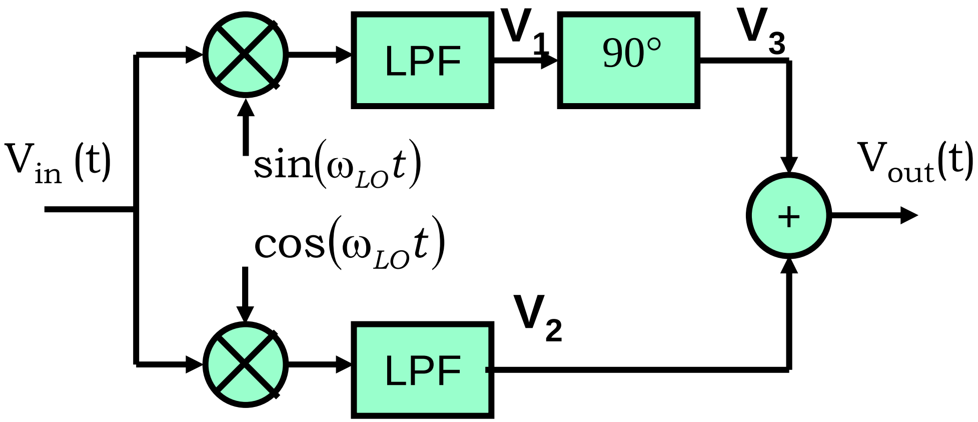
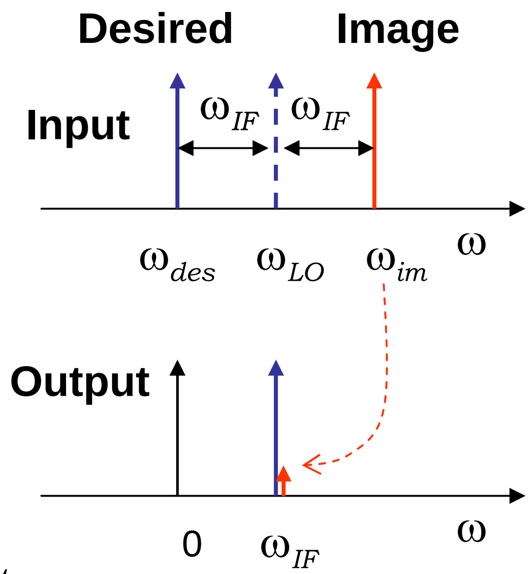


Image rejection mixer



$$V_1(t) = -\frac{V_{des}}{2}\sin(\omega_{des}-\omega_{LO})t + \frac{V_{im}}{2}\sin(\omega_{LO}-\omega_{im})t$$

$$V_2(t) = \frac{V_{des}}{2}\cos(\omega_{des}-\omega_{LO})t + \frac{V_{im}}{2}\cos(\omega_{LO}-\omega_{im})t$$

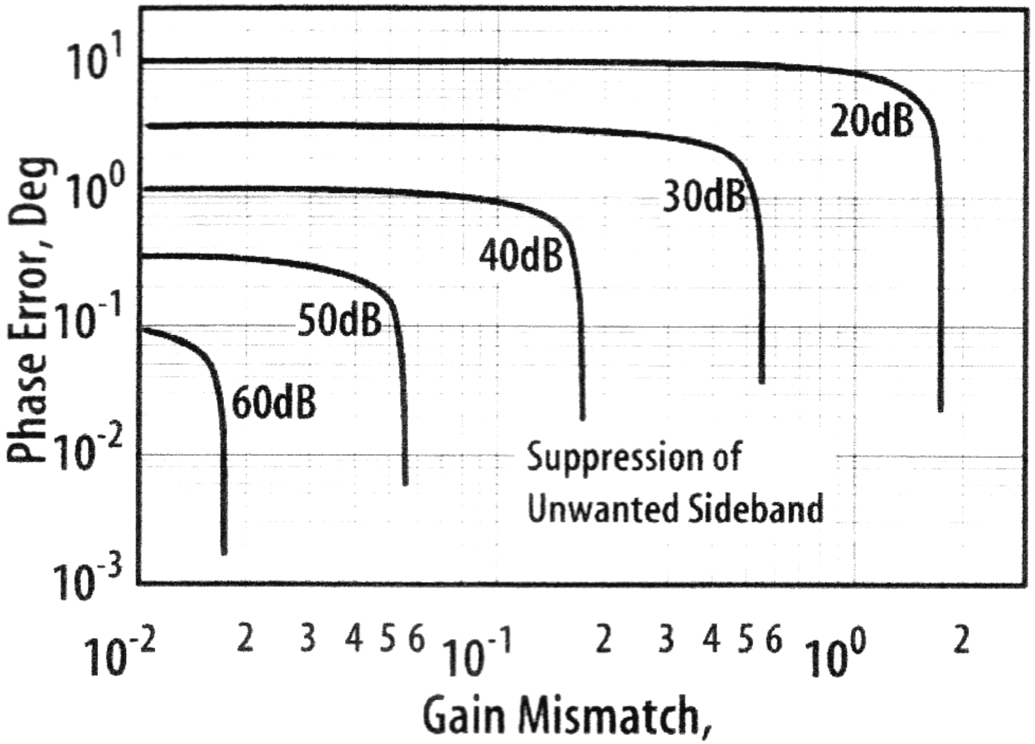
$$V_1(t) \rightarrow 90^\circ\ shift = V_3(t) = \frac{V_{des}}{2}\cos(\omega_{des}-\omega_{LO})t - \frac{V_{im}}{2}\cos(\omega_{LO}-\omega_{im})t$$

$$V_{out}(t) = V_{des}\cos(\omega_{des}-\omega_{LO})t$$

Image is rejected, however,…

Required gain and phase mismatch

0.1 deg and 0.01% are needed for IRR of 60dB



Conventional IRR: 35dB

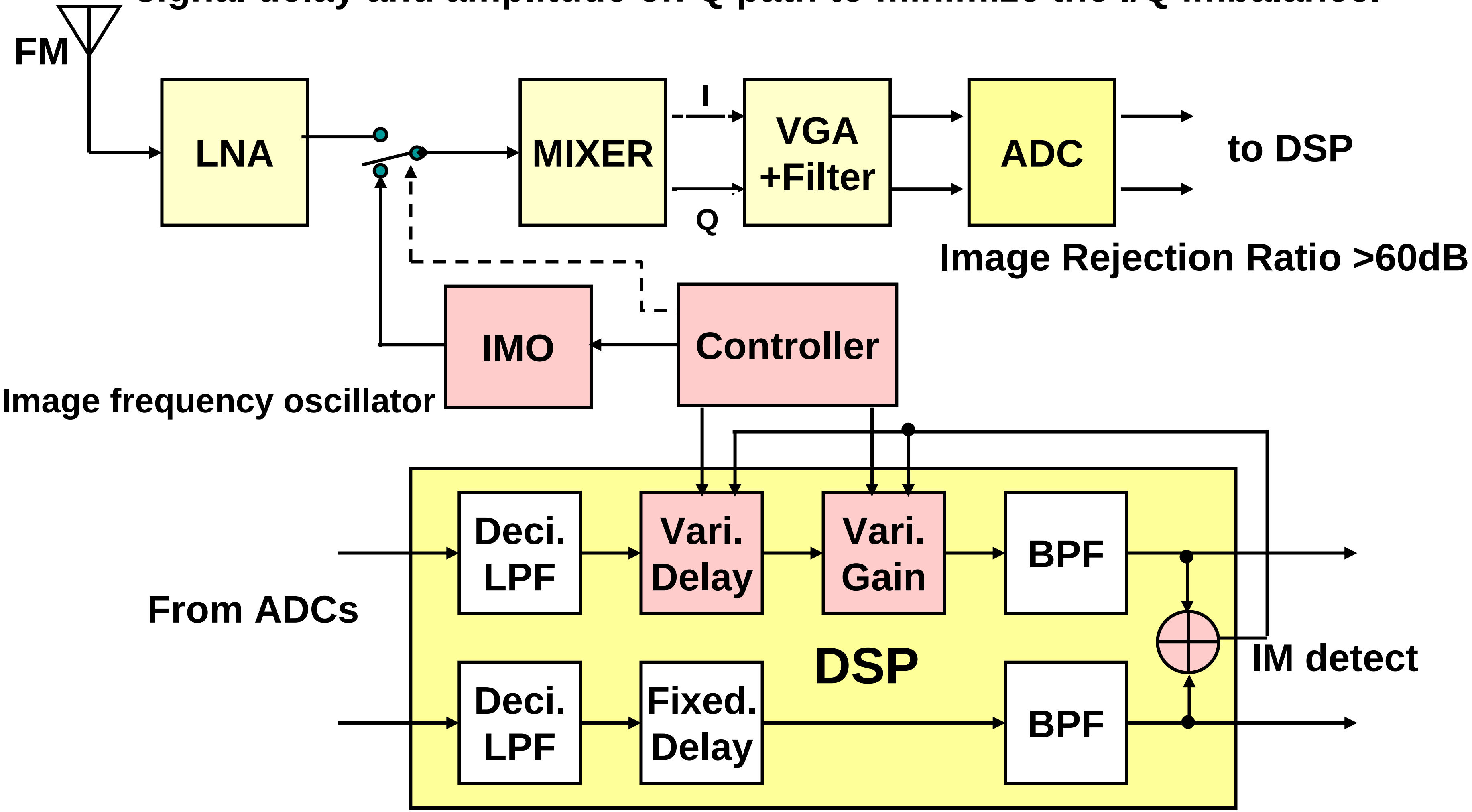
IRR: Image rejection ratio

$$IRR \approx \frac{\left(\frac{\Delta G}{G}\right)^2 + (\Delta\theta)^2}{4}$$

A. Rofougaran, et al.,
IEEE J.S.C. Vol.33, No.4,
April 1998. PP. 515-534.

Image rejection

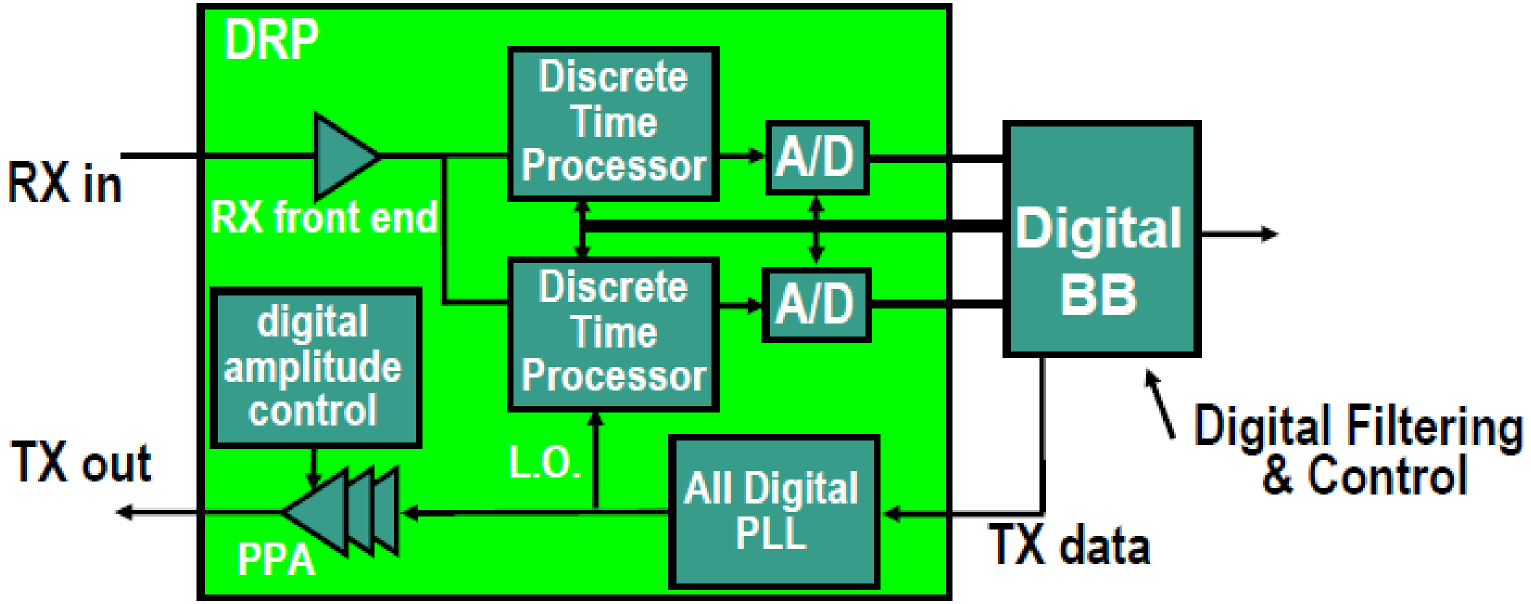
The dummy image signal is generated by IMO and the controller controls signal delay and amplitude on Q path to minimize the I/Q imbalance.



DRP: Digital RF Processing

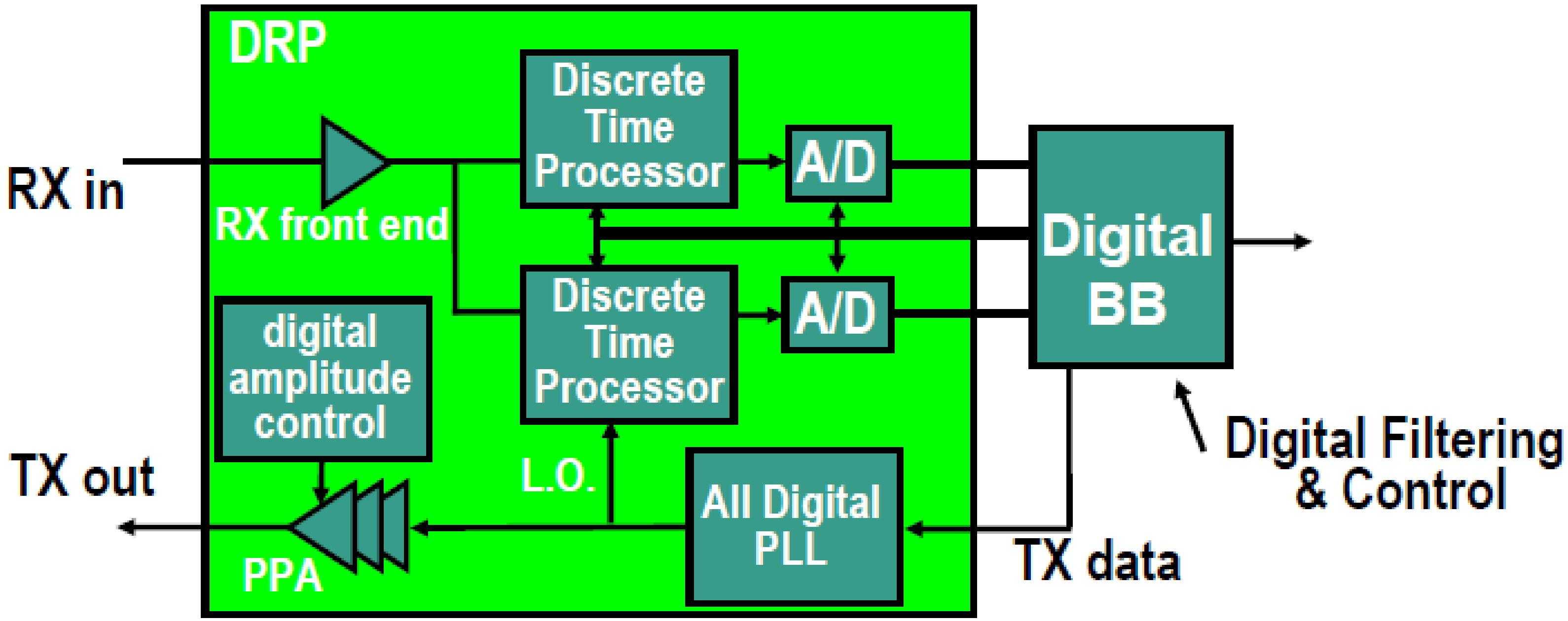
Courtesy Dr. R. B. Staszewski, TI

DRP approach for transceivers



- **Minimize analog and RF circuitry**
  - Self-calibrate remaining analog (with dedicated processor)
  - Relax passive requirements as much as possible
- **Digital approach speeds debug and development**
- **Self-test and calibration made possible**
- **Production yield dominated by silicon defect density**

DRP approach for transceivers



- **Move functions to domains of CMOS-process strengths**
  - Operate in fine time resolution, avoid fine voltage resolution
  - Inductor area could be equal to ~100K gates (use digital!)
  - Use switched cap techniques – excellent matching in DSM CMOS (not sensitive to process variations)
  - Logic and switched cap circuits can work well at low voltage

DRP Architecture

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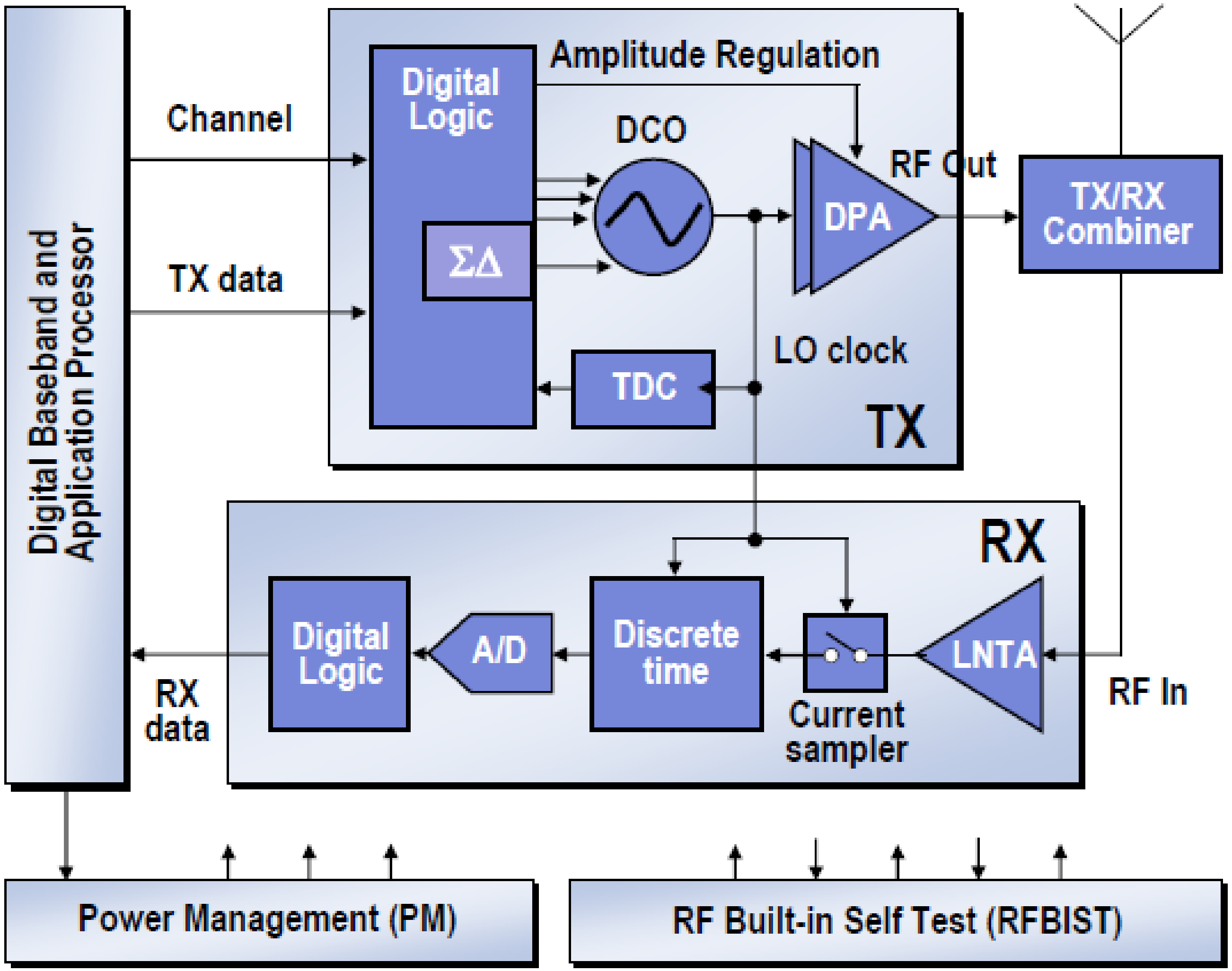


0.2, 1.25, 2.5,5, 10, 15, 20MHz BW

450, 800, 900, 1800, 1900, 2100, 2500, 3400MHz Transmission bands

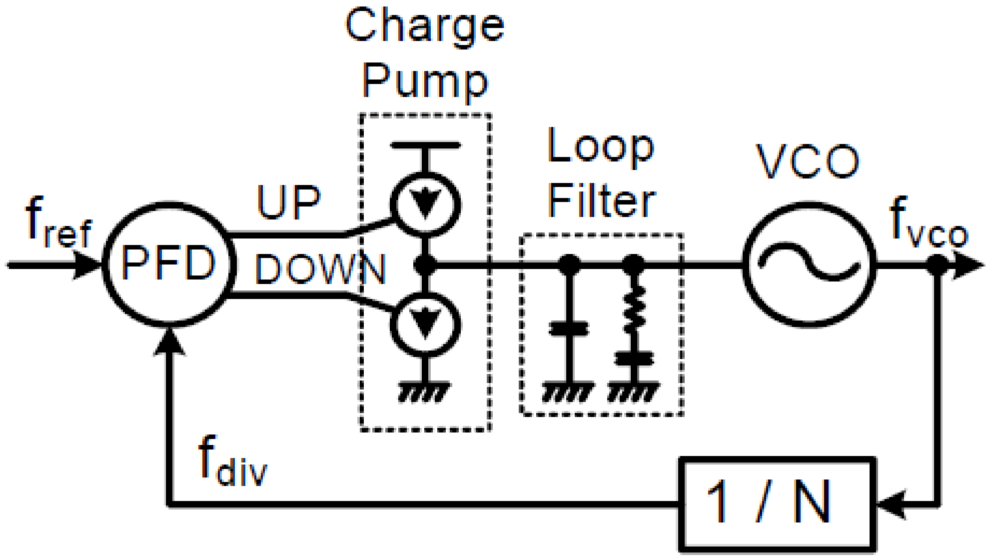
GMSK, QPSK, 8-PSK, 16QAM, 64QAM Modulation

TDMA, FDMA, CDMA, OFDMA, IFDMA schemes

Looks almost like SDR!!

Issues of conventional PLL

Performance of conventional PLL will degrade along with technology scaling.
Functions is not sufficient for future systems.



- Many analog functions = multiple noise sources
- Varactors in VCO are sensitive (high tuning factor, i.e. KVCO)
- Loop filter may be large, leaky capacitors (for open loop "freeze"), variances in passives…
- Hard to calibrate
- Lock times can be long (>100µsec)

All-Digital PLL

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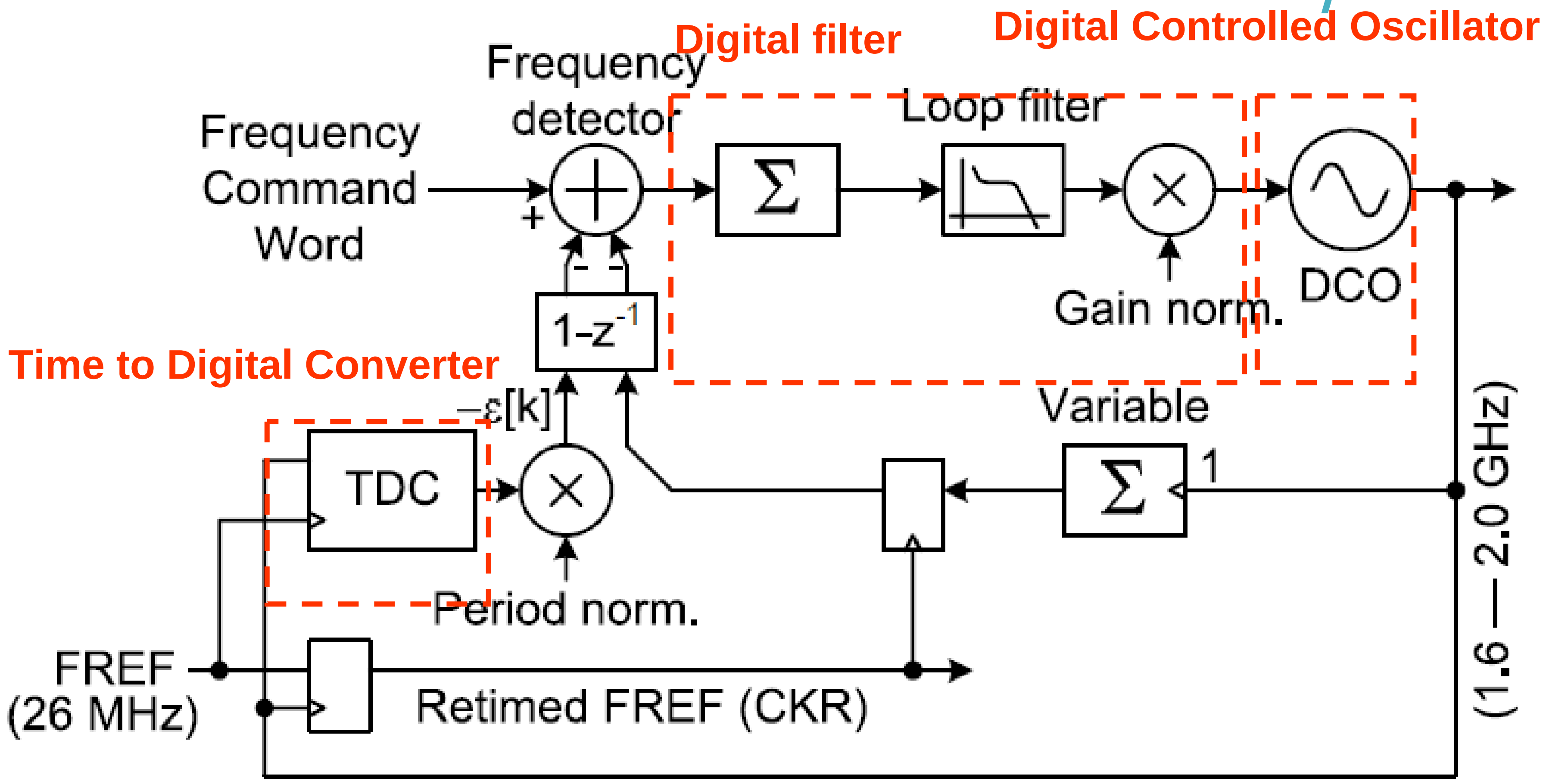
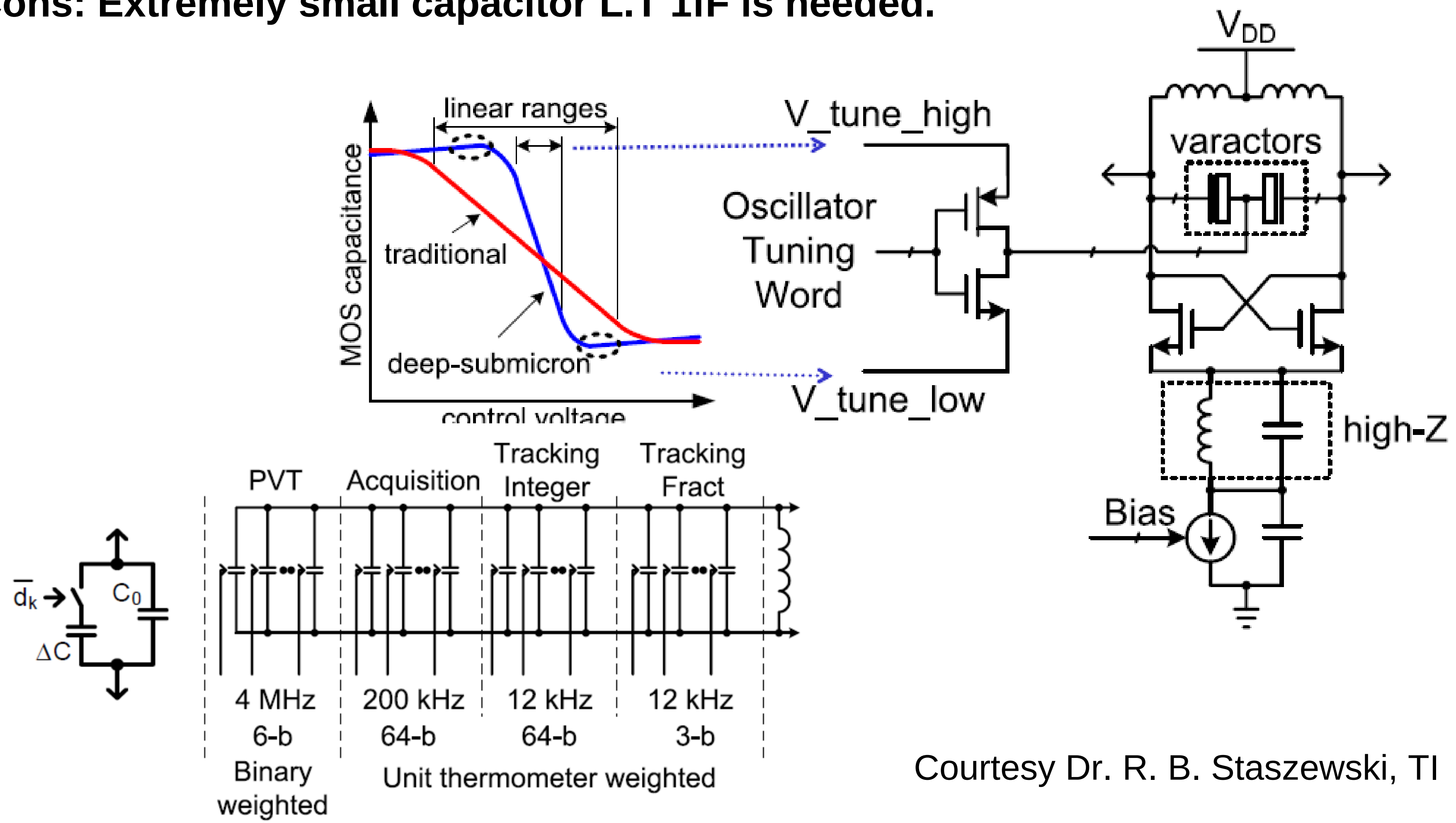


References [2], [3] - **R. Bogdan Staszewski et al.**

Matsuzawa & Okada Lab.

Digitally-controlled oscillator

Pros: Small effect to AM/PM conversion and noise on control voltage.
Cons: Extremely small capacitor L.T 1fF is needed.

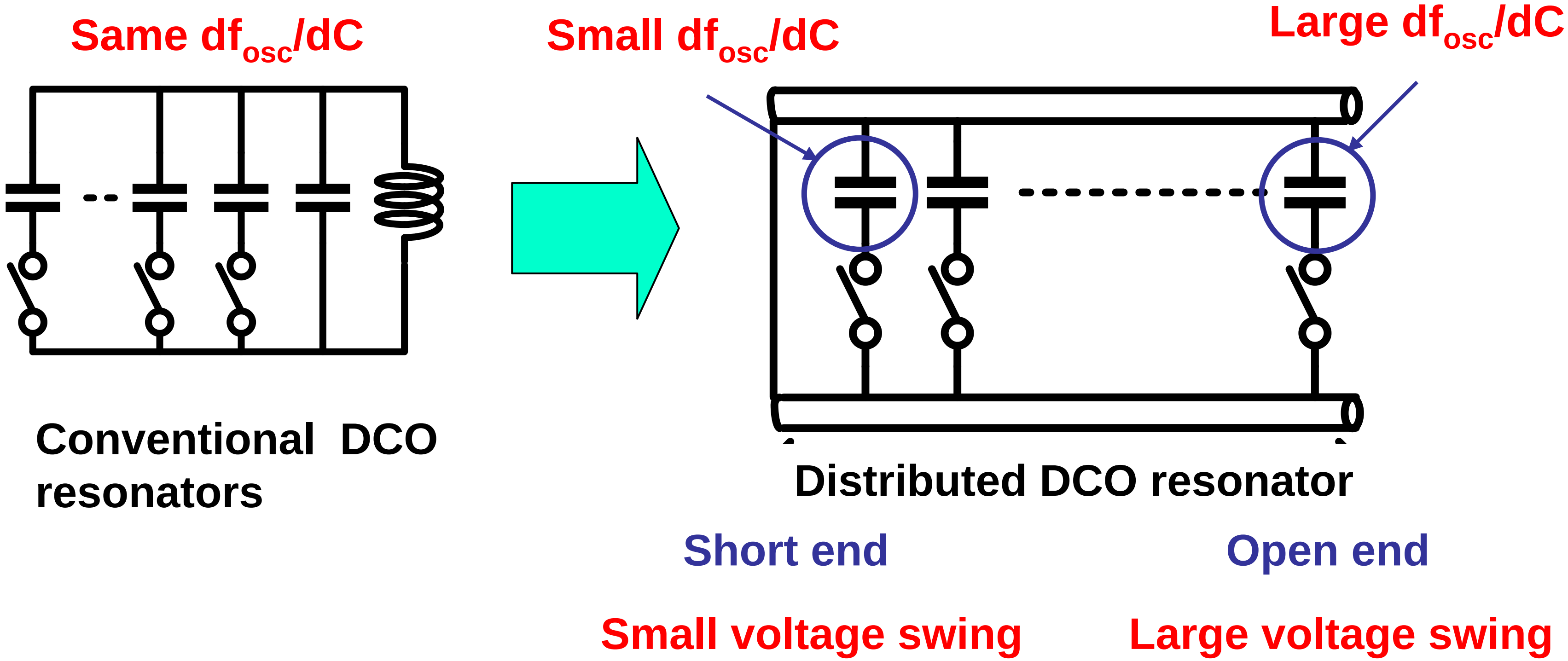


Courtesy Dr. R. B. Staszewski, TI

High-speed dithering and dynamic element matching are used to achieve high resolution (LSB = ~1.5Hz).

Proposed DCO

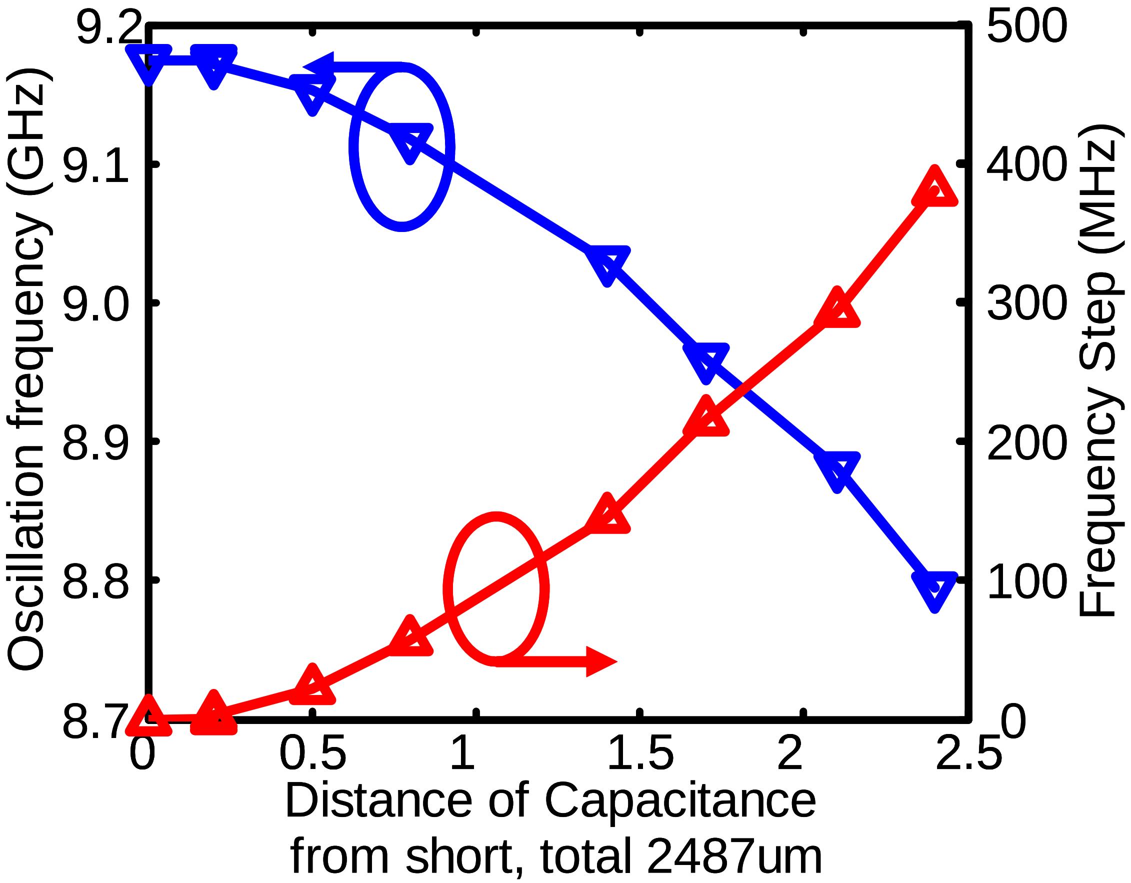
We proposed distributed DCO to realize fine frequency tuning with conventional capacitors



Win Chaivipas, Takeshi Ito, Takashi Kurashina, Kenichi Okada, and Akira Matsuzawa
"Fine and Wide Frequency Tuning Digital Controlled Oscillators
Utilizing Capacitance Position Sensitivity in Distributed Resonators"
A-SSCC, 16-1, pp 424-427, korea, jeju, Nov, 2007

Measured C to F_{osc} sensitivity

Over 100x capacitance to frequency sensitivity has been observed.



Outer Step C0
376 MHz

Inner Step C6
3.45 MHz

Min Step C7
<100kHz

TDC: Time-to-Digital Converter

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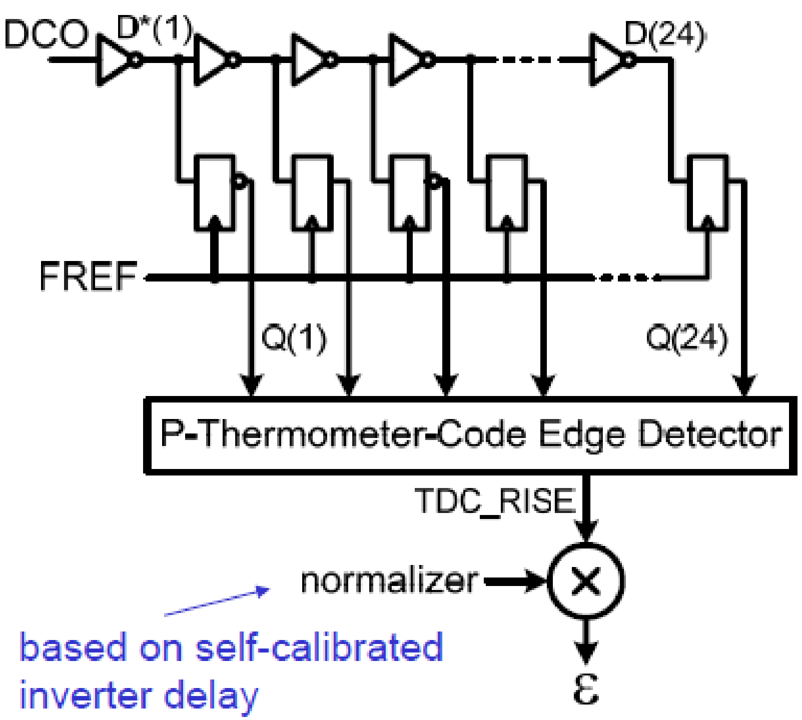
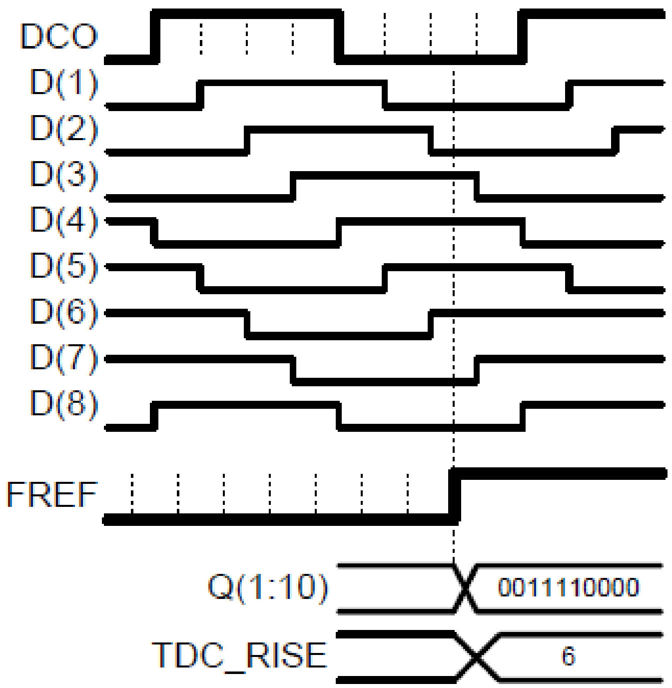
Issue: more small delay will be required.

- Quantized phase detector with resolution of about 20 ps
- DCO clock passes through the inverter chain
- Delayed outputs are sampled by FREF





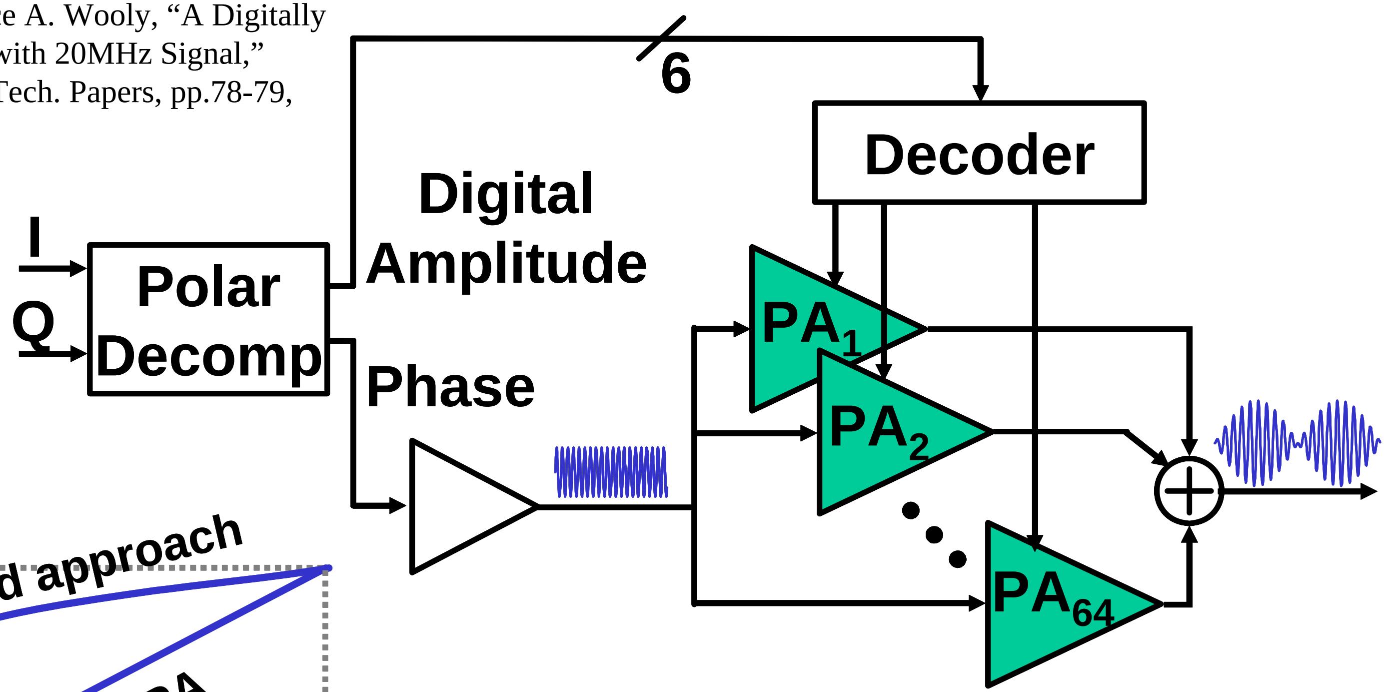
Matsuzawa & Okada Lab.

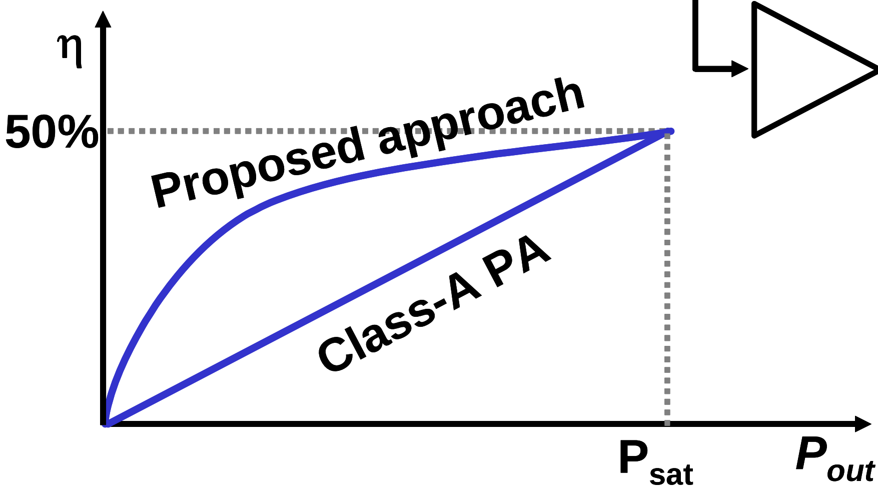
Digital polar modulation

Amplitude modulation has been realized by RF-DAC.

PA consists of DAC.

A. Kavousian, D. K. Su, Bruce A. Wooly, “A Digitally Modulated Polar CMOS PA with 20MHz Signal,” IEEE ISSCC 20007, Dig. of Tech. Papers, pp.78-79, Feb. 2007.





PA using DAC

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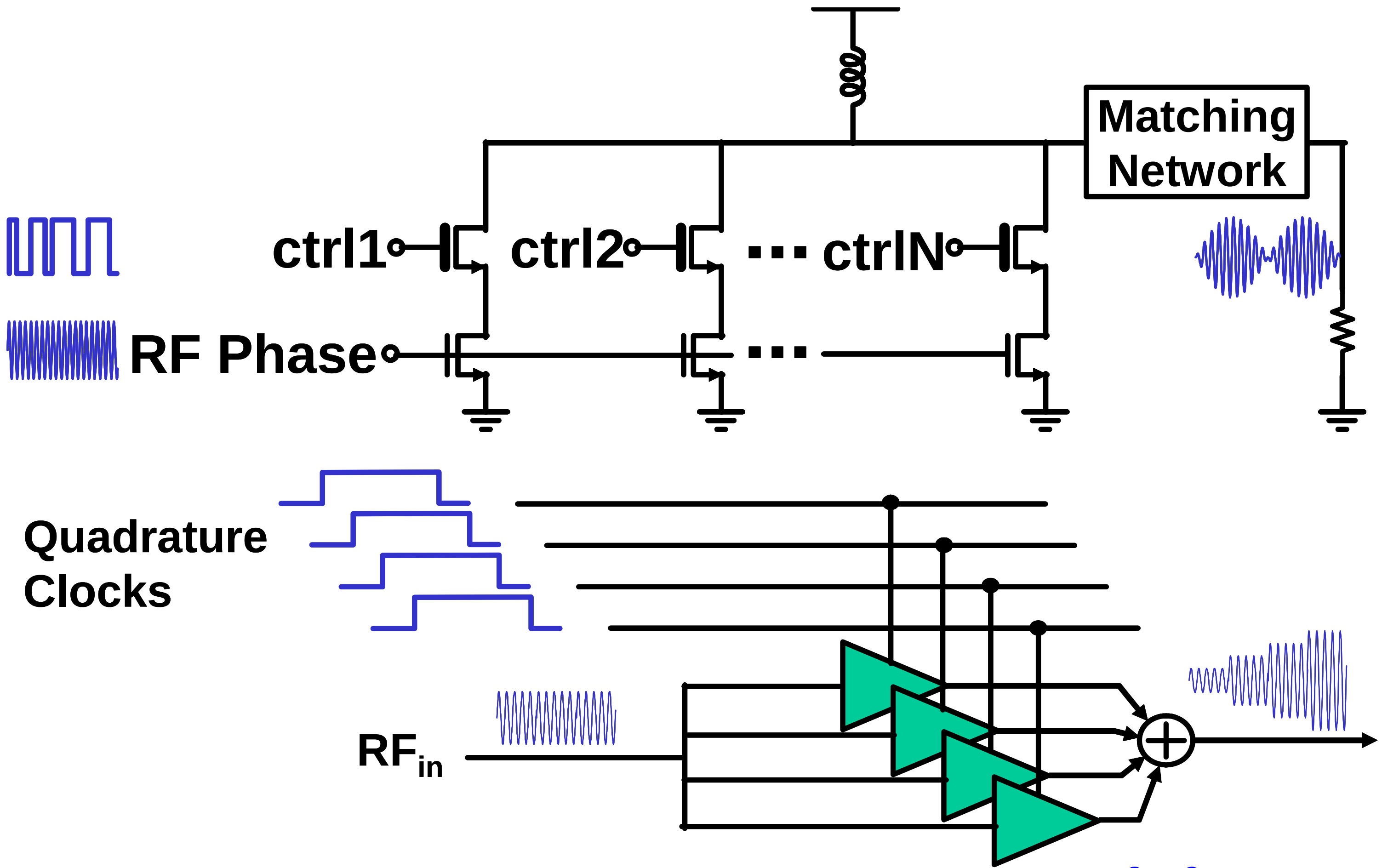
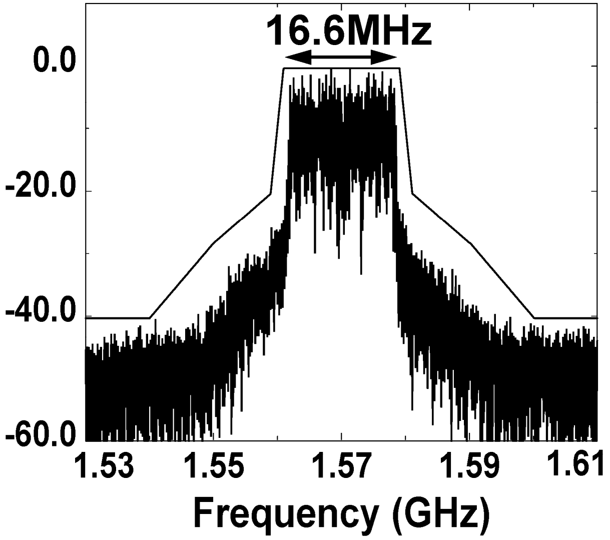
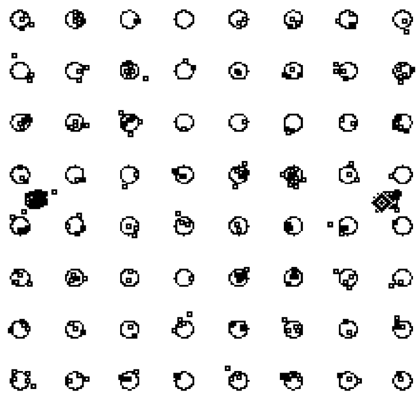
64 small PAs are controlled by digital BB signal.



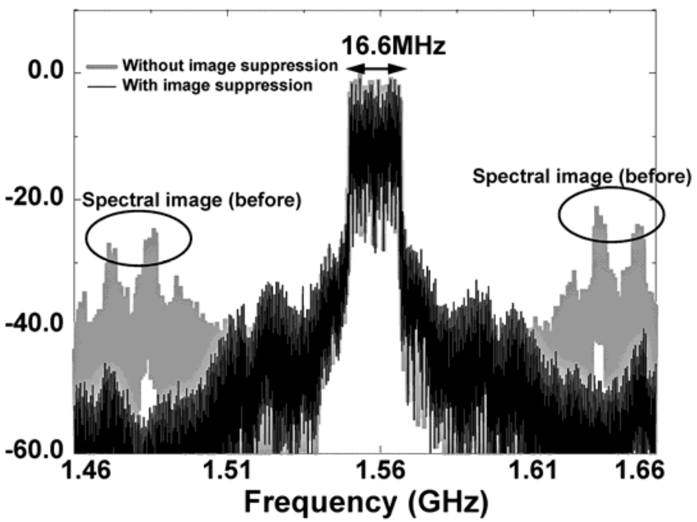
Results





EVM = -26.8dB

Po=13dBm
PAE=7.2%
BW=20MHz



Technology	0.18μm CMOS, 2P5M
Supply Voltage Digital Hardware Driver Stage Output Stage	 1.8V 2.2V 1.7V
Linear 64 QAM OFDM Output Power	14.7dBm 13.6dBm (balun included)
EVM for 64 QAM OFDM	–26.8dB
Dissipated Power Output Stage Driver Stage Digital	 247mW 66mW 3.4mW
PAE (for 64QAM OFDM)	8.9% 6.7% (baluns included)
Center Frequency	1.56GHz
Total Chip Area	$1.8mm^2$

サンプリングミキサー

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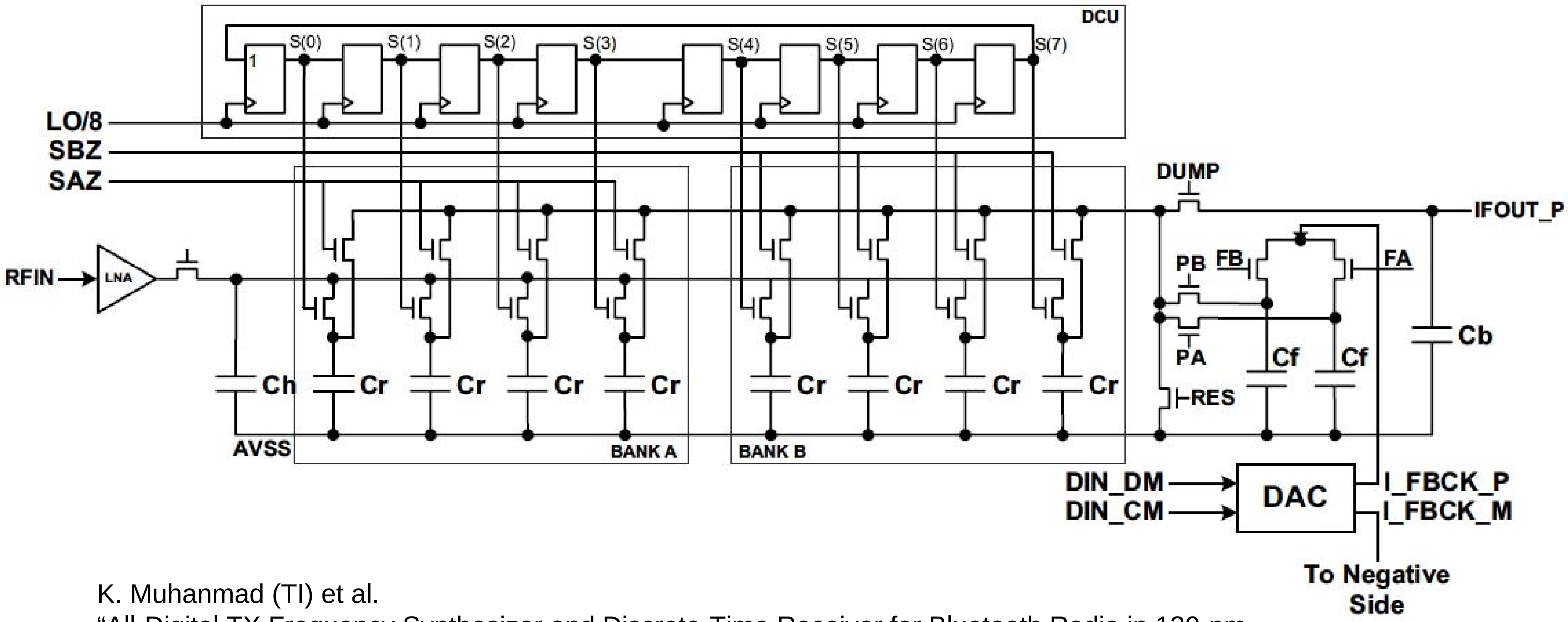
標本化回路はそれ自体ミキサー作用を持つが、容量アレーを用いて演算を行うことによりフィルター特性を持たせることができる。（離散時間信号処理のRF応用）
スイッチと容量という準受動回路で実現できるので、微細化に向いており、低電力である。



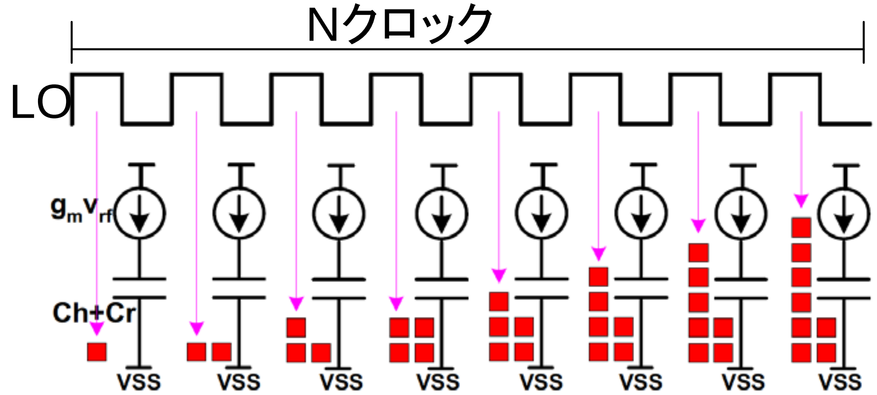
K. Muhanmad (TI) et al.
“All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS”
(JSSC Vol.39, No.12, pp. 2278-2291, Dec. 2004)

Matsuzawa & Okada Lab.

1st Sinc Filter

- LOクロックN回の移動平均

$$w_i = \sum_{l=0}^{N-1} u_{i-l}$$



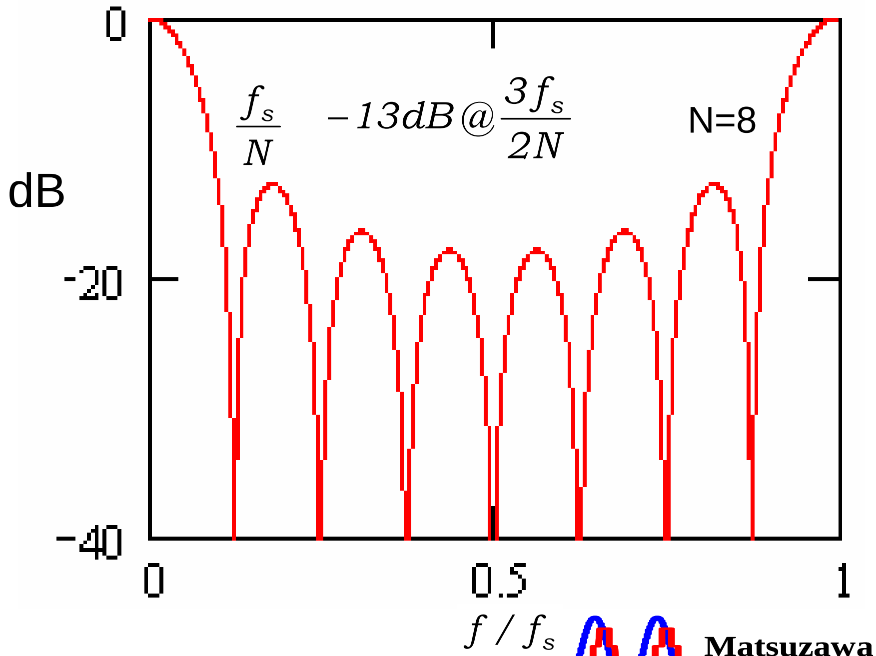
ui： i番目にサンプリングされた電荷

wi： Nクロックの間に蓄積された電荷

$$w_i = \sum_{l=0}^{N-1} u_{i-l}$$

$$\rightarrow W(Z) = \frac{1 - Z^{-N}}{1 - Z^{-1}} U(Z)$$

$$\rightarrow \left|F_{1stSinc}(\omega)\right| = \left| \frac{\sin\left(N\pi \frac{f}{f_s}\right)}{\sin\left(\pi \frac{f}{f_s}\right)} \right|$$



1^{st} IIR Filter

- 電荷がC_hとC_rに分割して蓄積される

$$s_j = as_{j-1} + w_j \xrightarrow{i=Nj} s_i = as_{i-N} + w_i$$

$$a = \frac{C_h}{C_h + C_r}$$

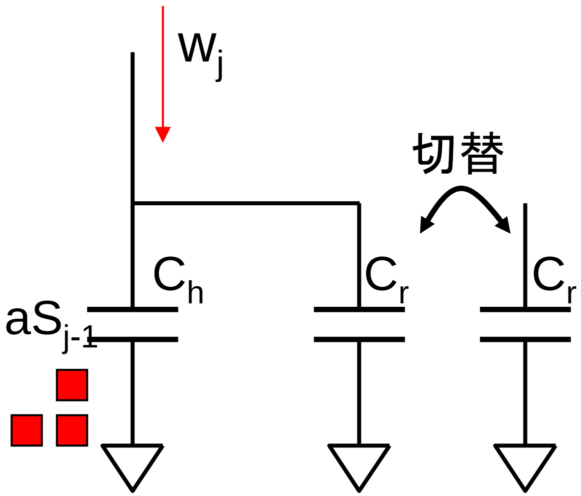
aS_{j-1} : j-1のときC_hに蓄積された電荷

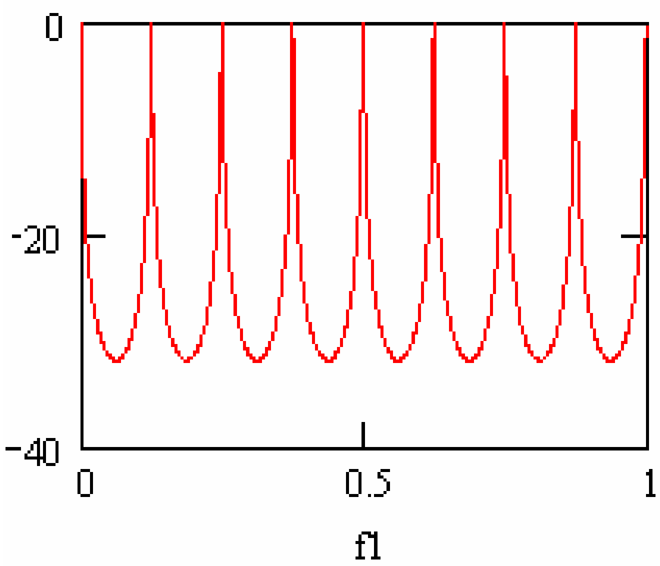
W_j : jのときC_hとC_r注入された電荷

S_j : jでC_hとC_rに蓄積されている電荷の合計

$$s_i = as_{i-N} + w_i \rightarrow S(Z) = \frac{W(Z)}{1 - aZ^{-N}}$$

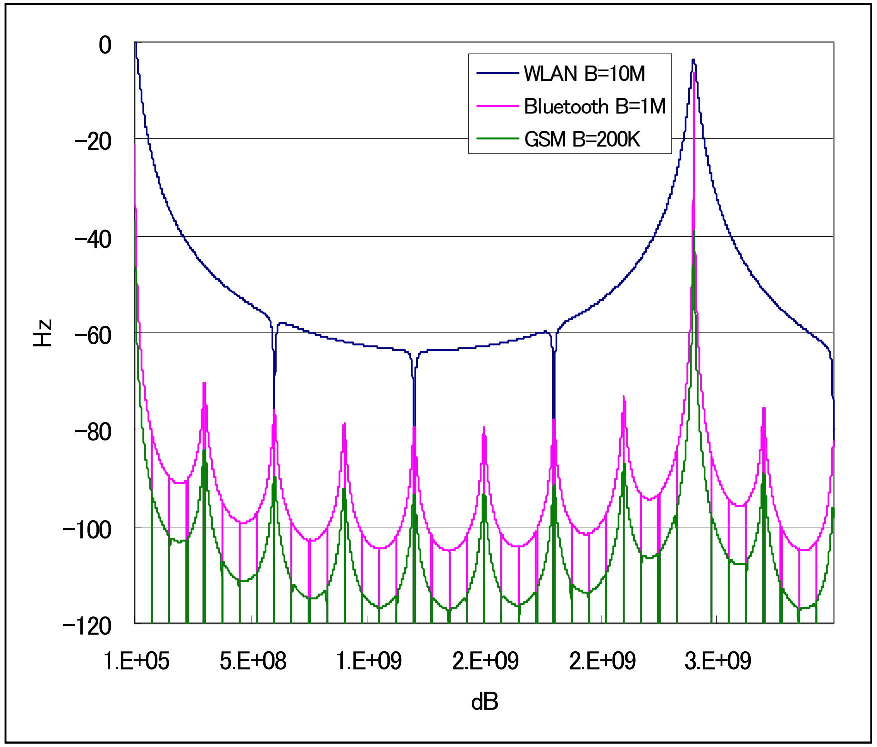
$$\rightarrow \left|F_{1stIIR}(f/f_s)\right| = \frac{1}{\sqrt{1 + a^2 - 2a\cos\left(N2\pi\frac{f}{f_s}\right)}}$$

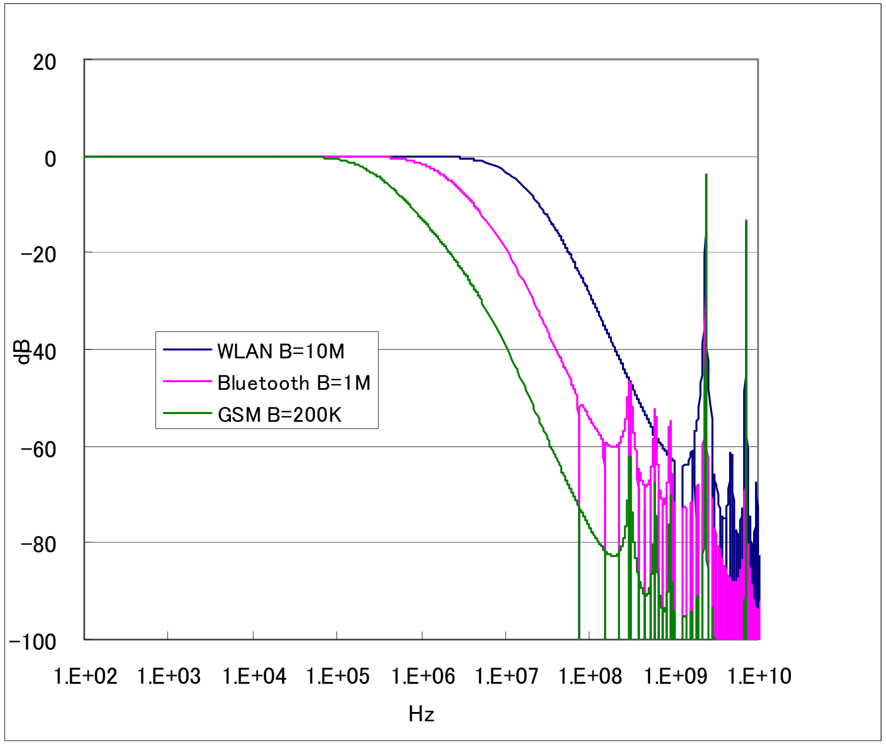




フィルター特性の可変化

容量比や平均化回数などを変えることによりフィルター特性を可変にできる

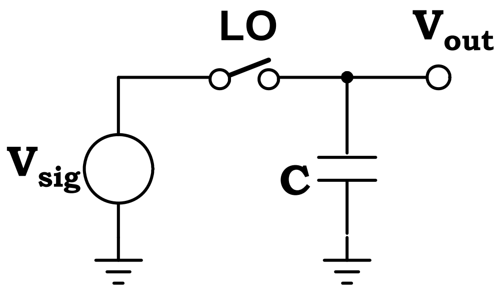




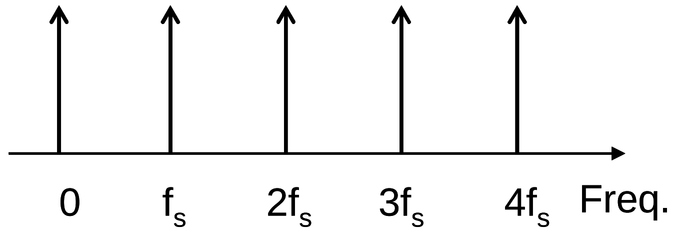
Sampling mixer vs. switch mixer

Switch mixer has almost same frequency characteristics as sampling mixer.

Voltage sampling

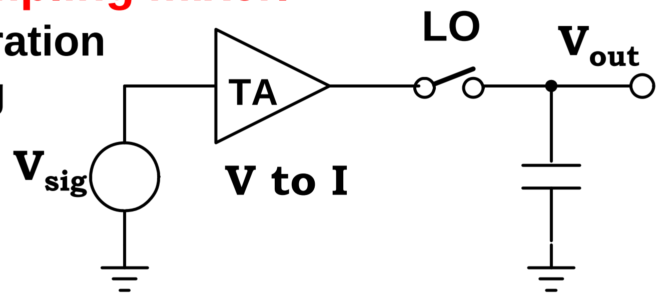


Can't use, because of large aliases

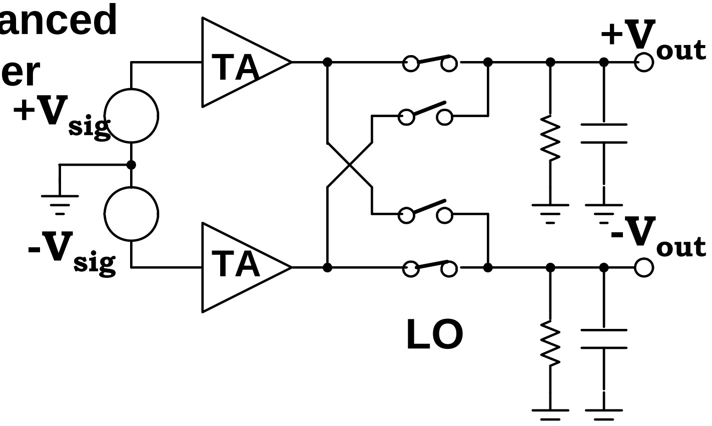


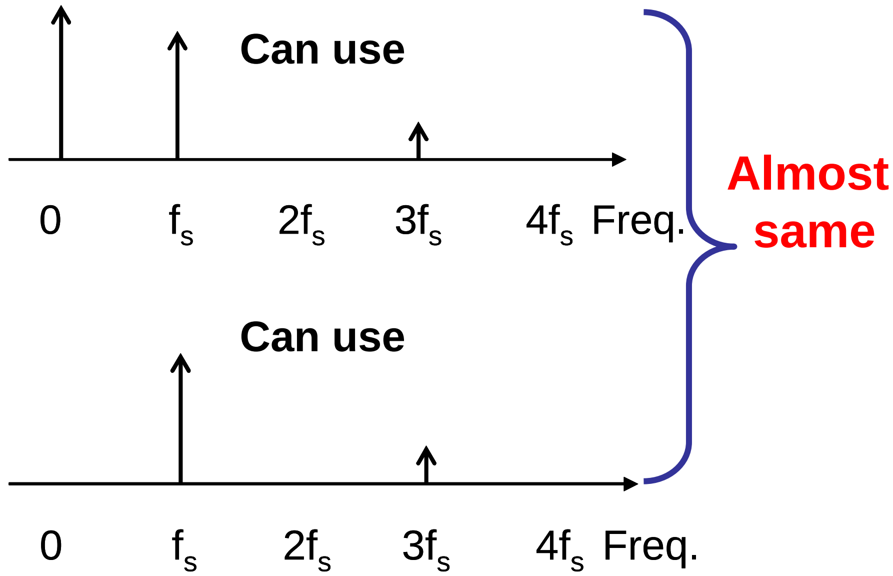
This is a sampling mixer.

Current integration and sampling



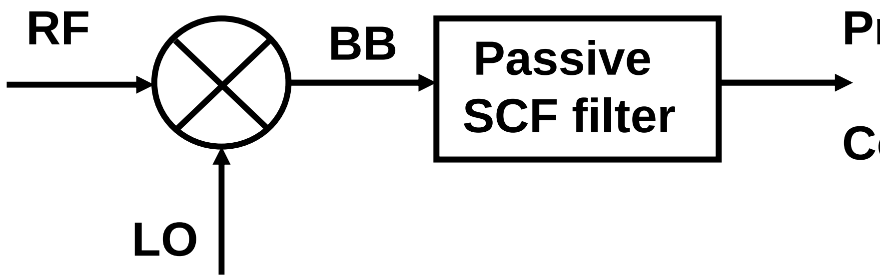
Double balanced Switch mixer





Passive SCF filter vs. CT filter

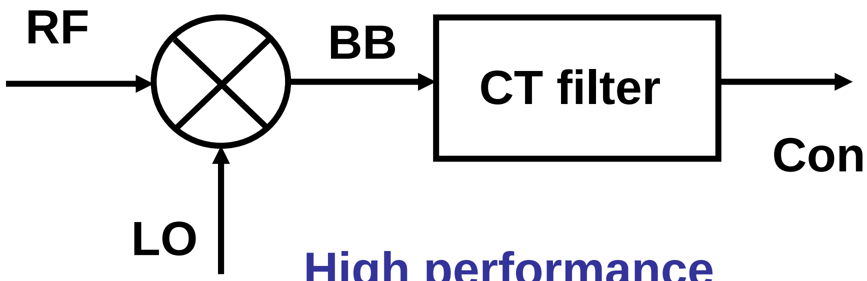
Passive SCF filter looks less attractive, so far.



Pros: Low power

Cons: Poor SNR
Still needs an anti-alias filter
Narrow band and low filter order
Restricted operating frequency

Poor performance
Not suitable for reconfigurability



Pros: No needs an anti-alias filter
Wider band and higher order

Cons: consumes power

High performance
Suitable for reconfigurability

Conclusion

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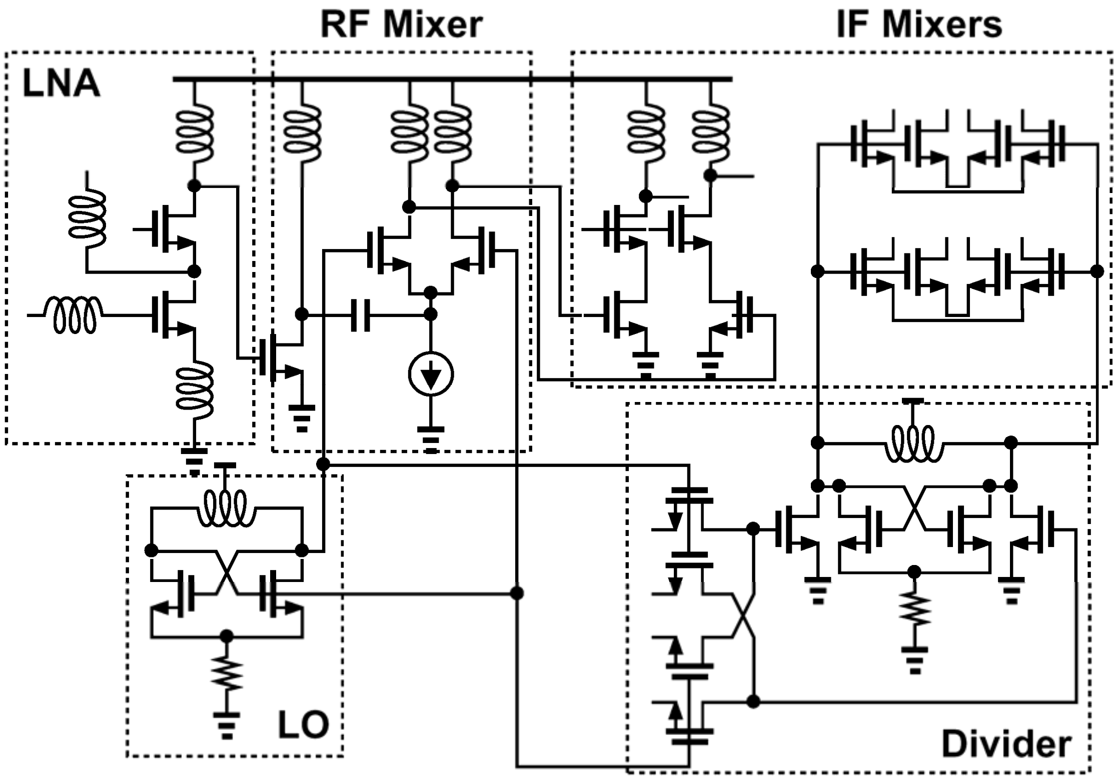
- **Analog-centric CMOS technology will go away**
  - No attractive performance and affected by PVT fluctuation seriously.
  - Cost increase for further technology scaling
  - Still need large # of external components and adjusting points
- **Digital-centric CMOS technology must be right way**
  - High performance and very robust against PVT fluctuations
  - Further performance increase and cost reduction are expected by using more scaled technology
  - No or less external components and no adjustment points
- **Digital-RF technology sounds interesting, however not matured yet.**
  - Performance is not attractive

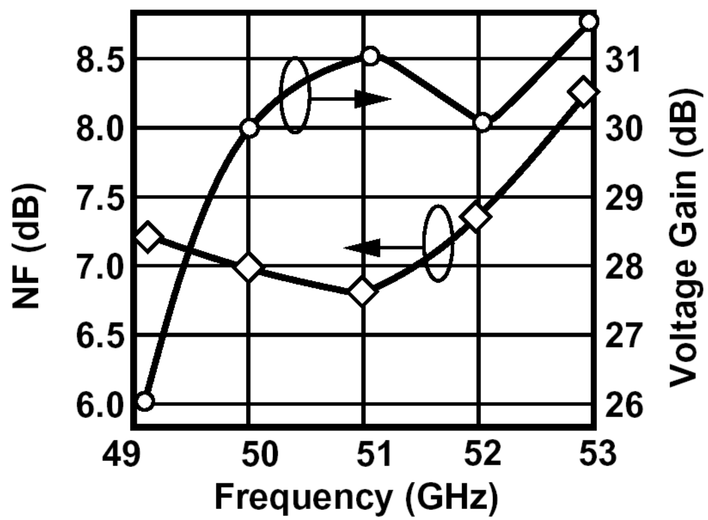
mm-wave SoCs

60GHz ミリ波CMOSレシーバー 1

90nm CMOSを用いて60GHzのレシーバーを実現



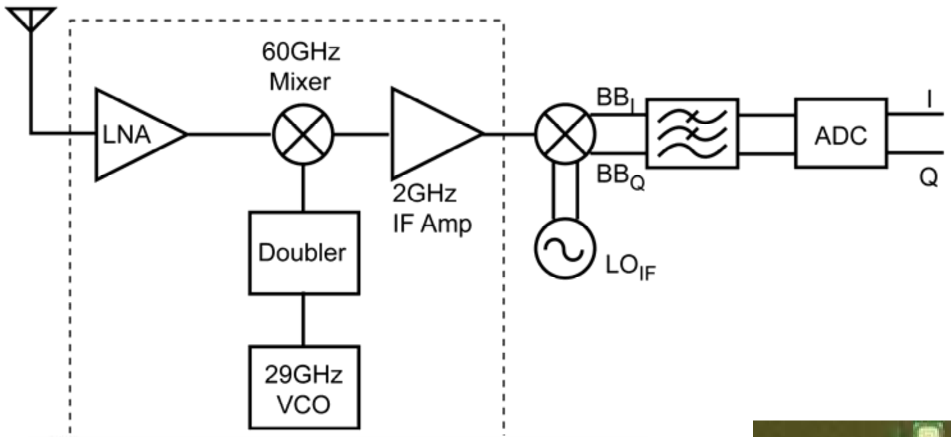
B. Razavi"A mm-Wave CMOS Heterodyne Receiver with On-Chip LO and Driver," IEEE ISSCC 20007, Dig. of Tech. Papers, pp.188-189, Feb. 2007.

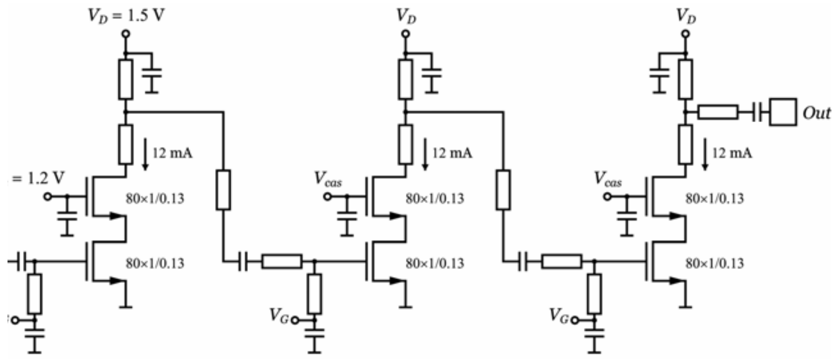


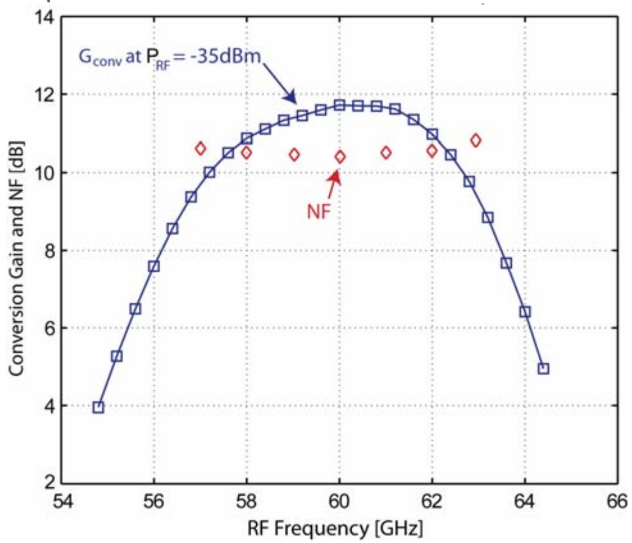
60GHz ミリ波CMOSレシーバー 2

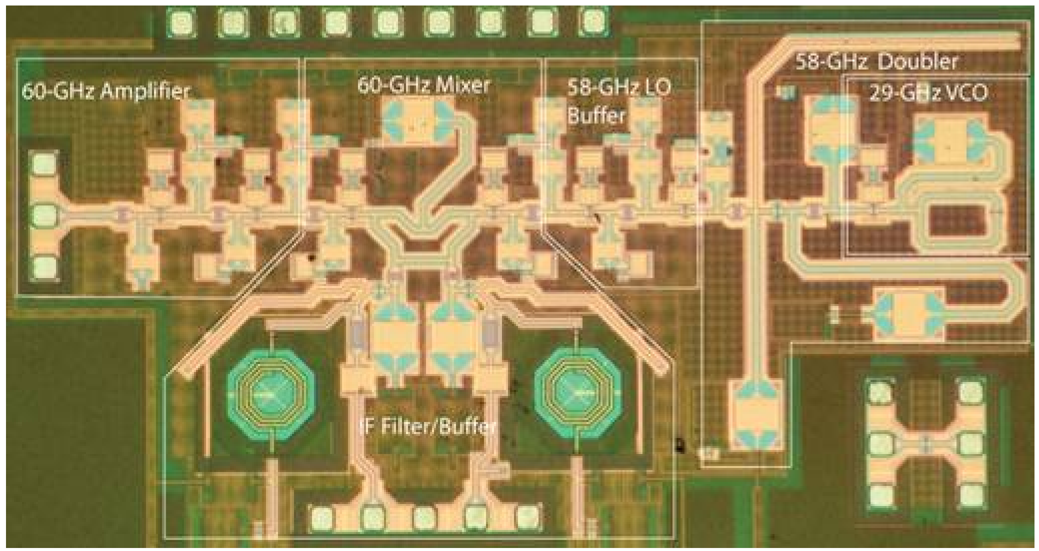
0.13um CMOSを用いても60GHzのレシーバーが実現できる

S. Emami, C. H. Doan, A. M. Niknejad, R. W. Broderson, “A Highly Integrated 60GHz CMOS Front-End Receiver,” IEEE ISSCC 20007, Dig. of Tech. Papers, pp.180-191, Feb. 2007.



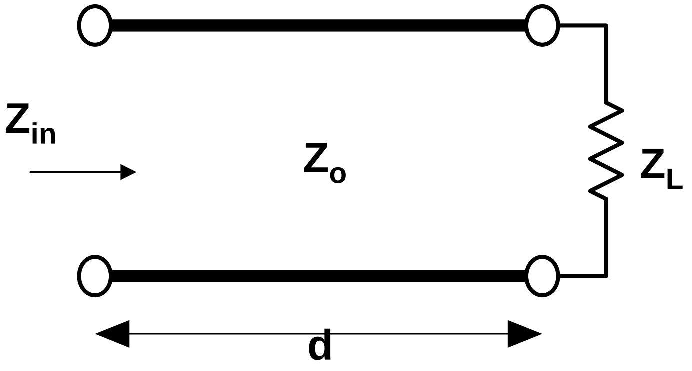






トランスミッションラインの応用

ミリ波では波長が短いためトランスミッションラインが使用できる。
インピーダンス整合や共振器、発振器として使用できる。

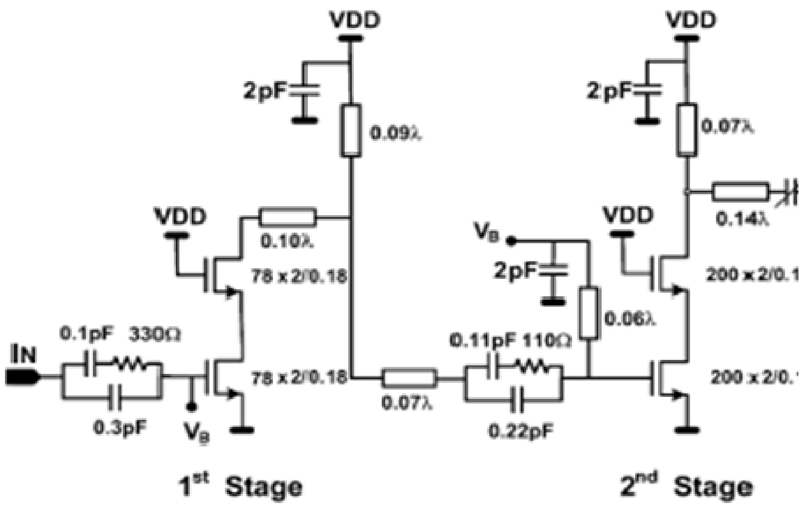


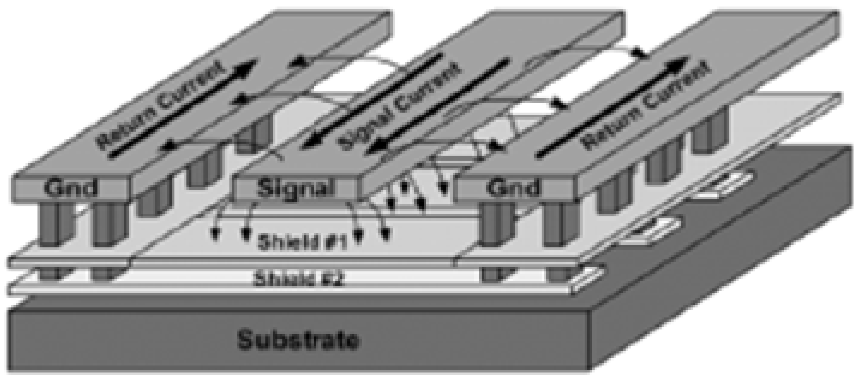
$$Z_{in} = Z_0 \frac{Z_l + jZ_0 \tan\beta d}{Z_0 + jZ_l \tan\beta d}$$

$$Z_{in}\left(\frac{\lambda}{4}\right) = \frac{Z_0^2}{Z_l}$$

resonator

$$Z_{in}\left(\frac{\lambda}{4}\right) = \infty \quad when\ Z_l = 0$$





Coplanar transmission line

ミリ波フェーズドアレーシステム

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ミリ波では波長が数mmになるので、チップ上にアンテナを集積することが可能

給電位相の変化により電子的にビームフォーミング可能

オンチップ上に4つのアンテナを配置

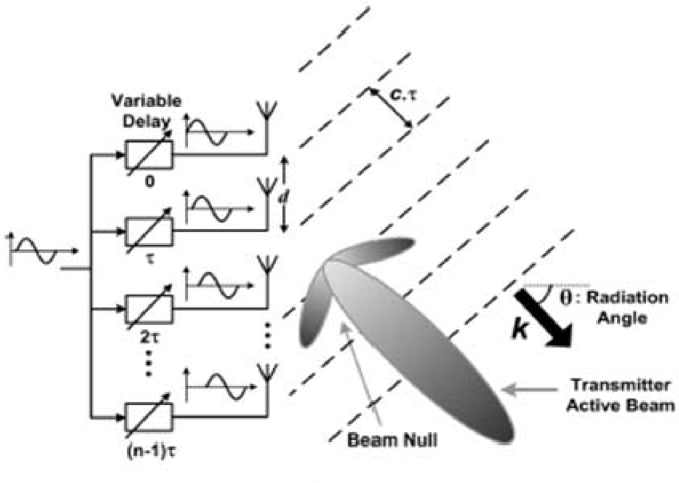
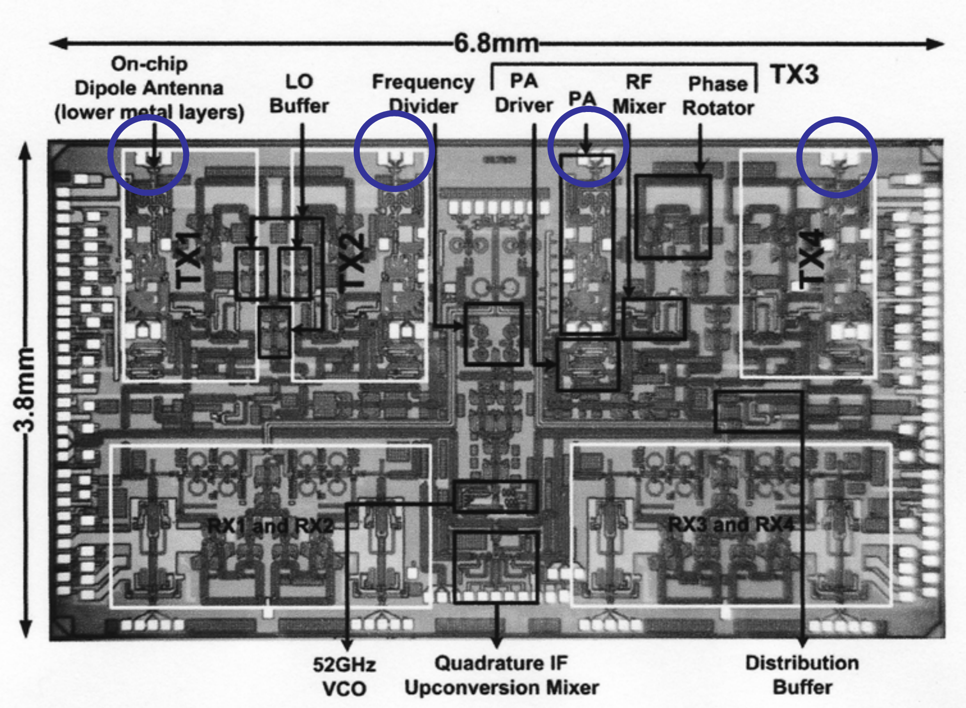


Fig. 1. n-element phased-array transmitter.



A. Natarajan, et. al., IEEE, Journal of Solid-State Circuits, Vol. 40, No. 12, pp. 2502-2514, Dec. 2005.
A. Natarajan, et. al., IEEE, Journal of Solid-State Circuits, Vol. 41, No. 12, pp. 2807-2819, Dec. 2006.

ビームフォーミング

ビームフォーミングは信号強度を上げ、伝送レートを速くするためにも有効

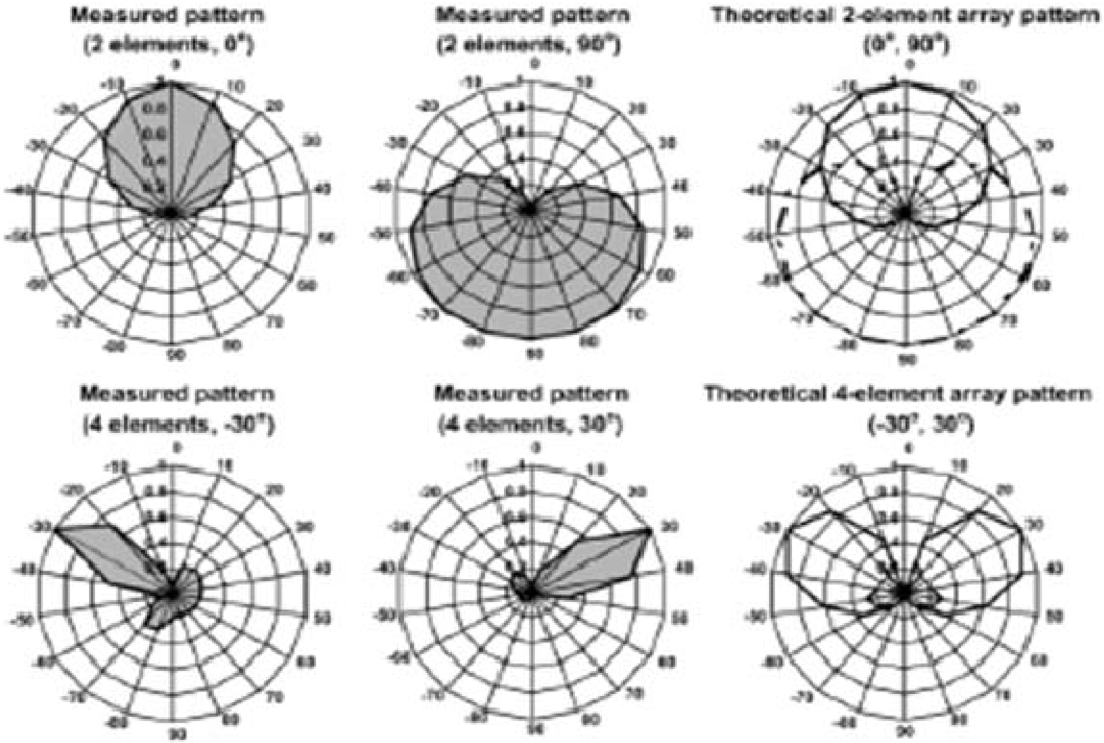


Fig. 21. Comparison of theoretical and measured array pattern with two elements and with four elements active.

レンズの集積

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77GHzのミリ波トランシーバ：オンチップアンテナとレンズを集積

10.1 A 77GHz 4-Element Phased Array Receiver with On-Chip Dipole Antennas in Silicon

0.13um SiGe-CMOS

A. Babakhani, X. Guan, A. Komijani, A. Natarajan, A. Hajimiri

California Institute of Technology, Pasadena, CA

IEEE ISSCC 2006, Dig. Technical Papers, pp.180-181.

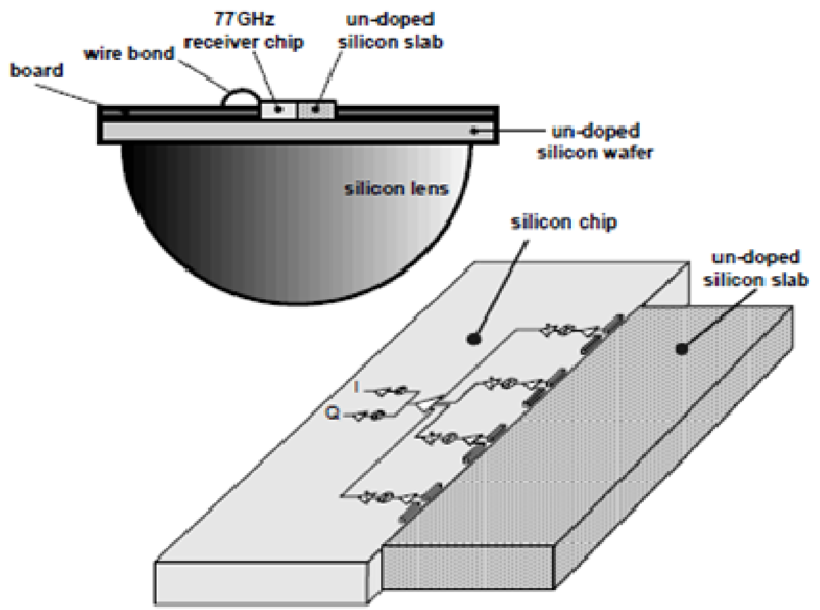


Figure 10.1.1: Chip, board, and lens antenna setup configuration.

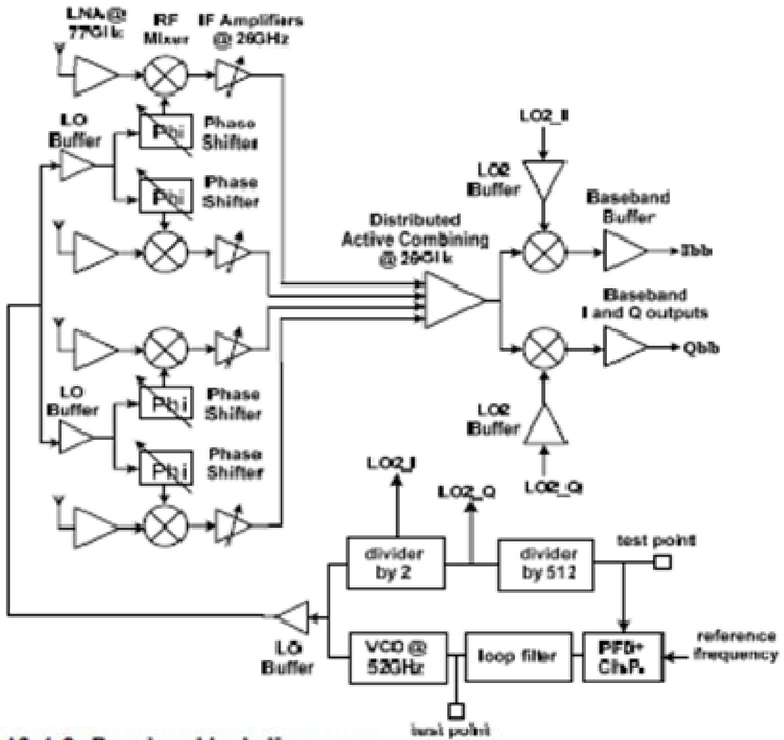
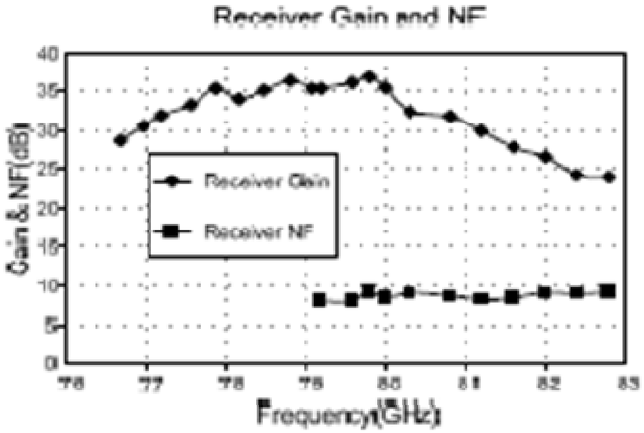


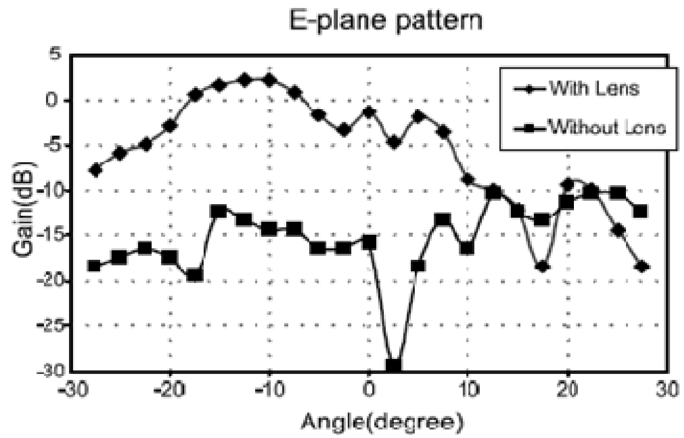
Figure 10.1.3: Receiver block diagram.

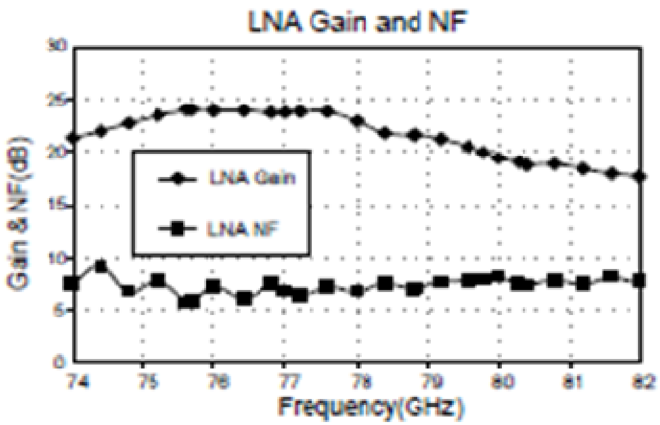
Matsuzawa & Okada Lab.

性能

レンズを用いることにより10数dBの感度アップ







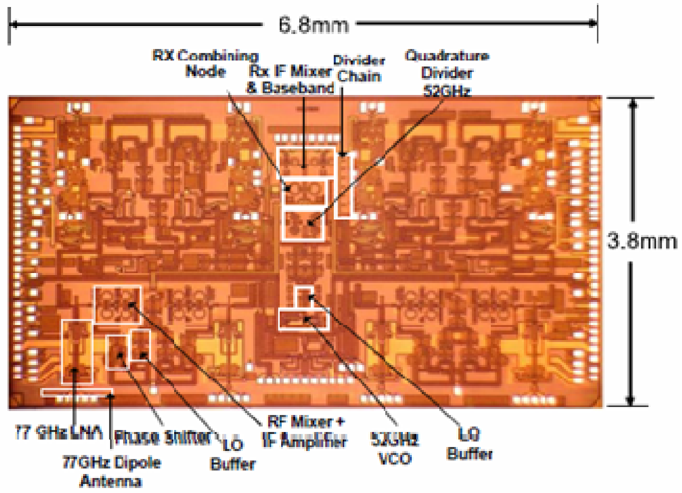
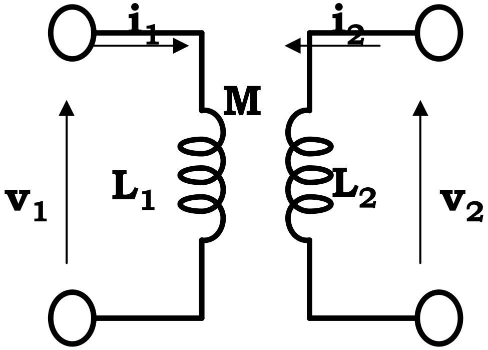


Figure 10.1.7: Chip micrograph.

近接磁気結合

磁気結合により高速・低電力データ伝送が可能。

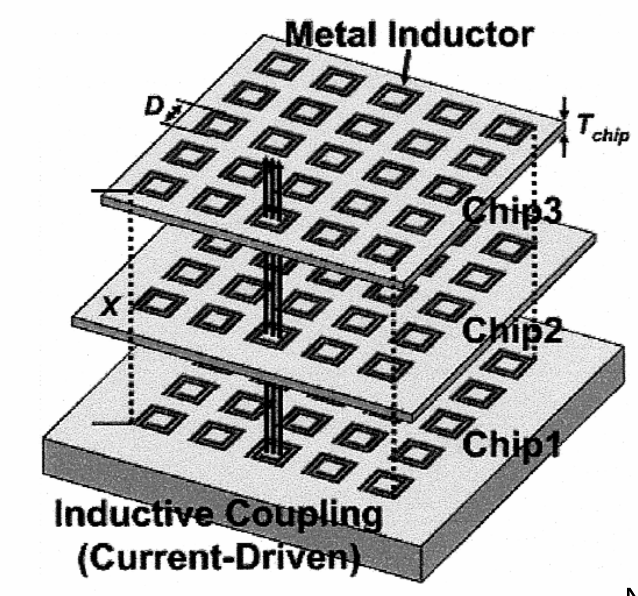


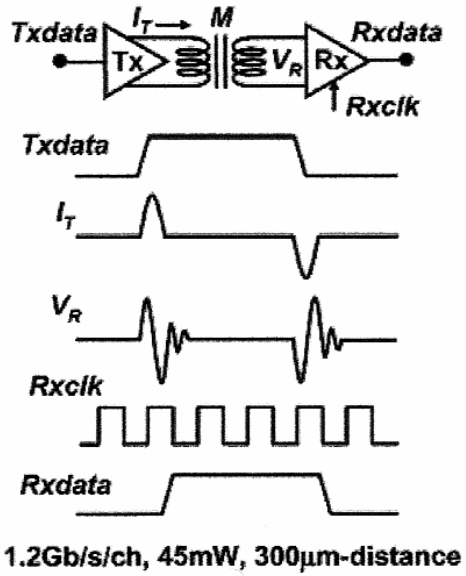
$$v_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$$

$$v_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt}$$

$$v_2 = M \frac{di_1}{dt}$$

$$M \propto \frac{\sqrt{L_1 L_2}}{x^3}$$





N. Miura, et. al., IEEE, JSC, Vol. 41, No. 1, pp. 23-34, Jan. 2006.

近接磁気結合

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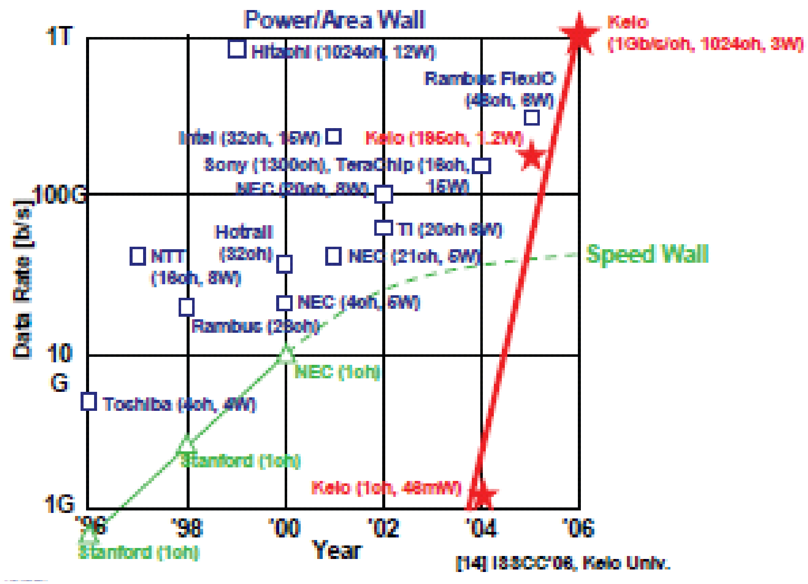
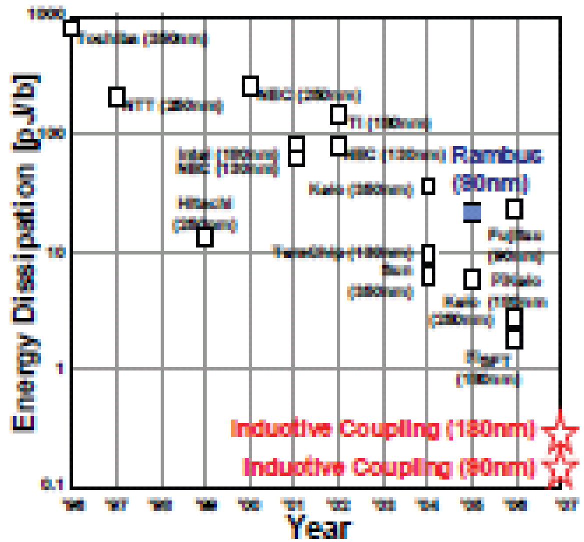
スタックされたLSI間の高速データ通信に有効である。

Data rate: 1Gbps/ch
Energy consumption:140fJ/b

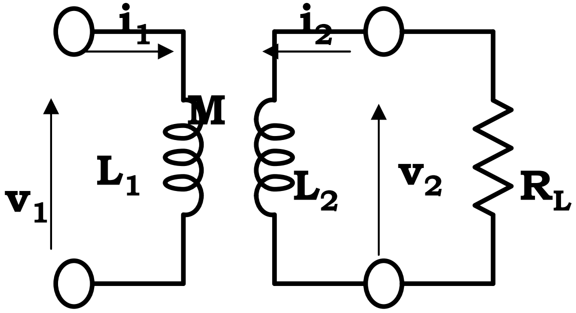




Matsuzawa
& Okada Lab.

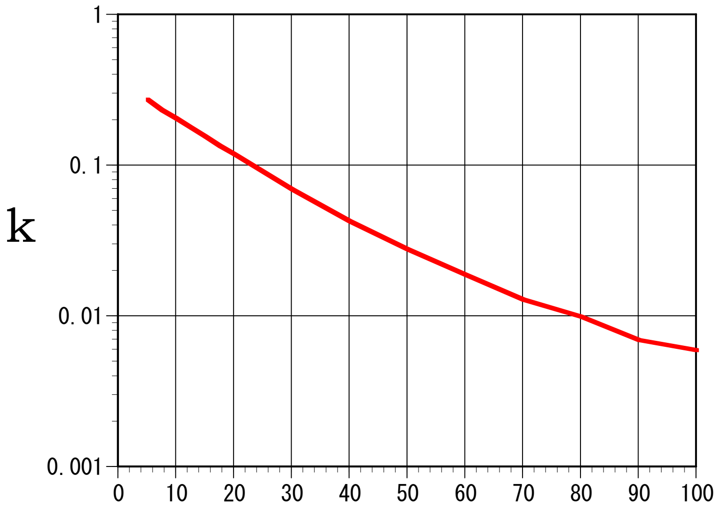
磁気結合による電力の伝送

磁気結合により データのみならず電力を送ることができる。
体内チップへの応用などが期待される。

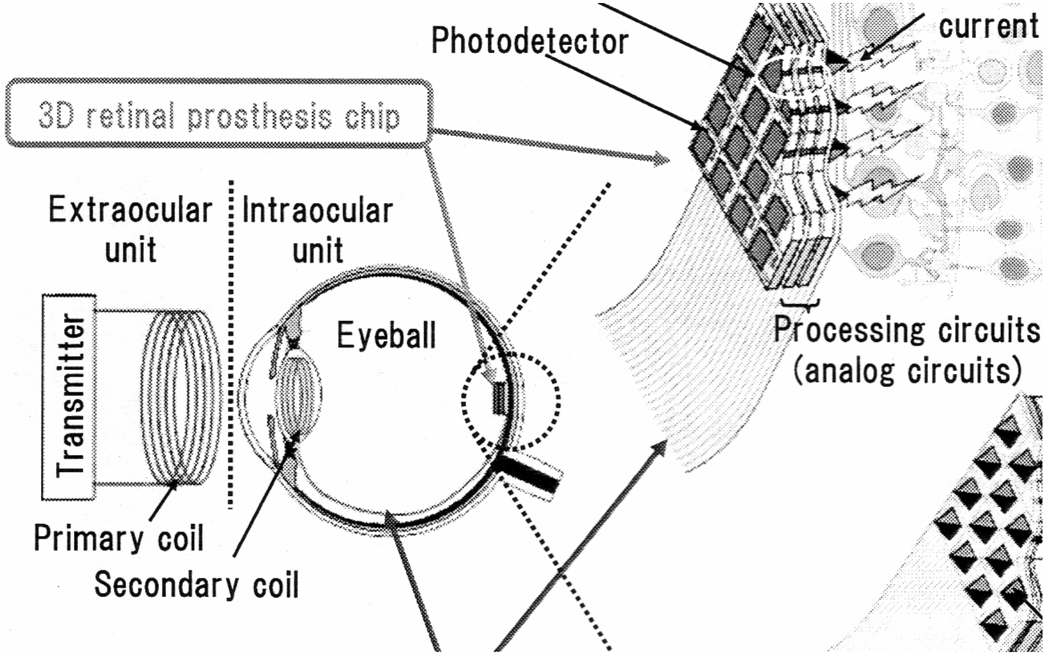


$$P_L = k^2 \frac{L_1}{L_2} I_1^2 R_L \quad k = \frac{M}{\sqrt{L_1 L_2}} \propto \frac{1}{d^3}$$

K decreases rapidly with increase of distance



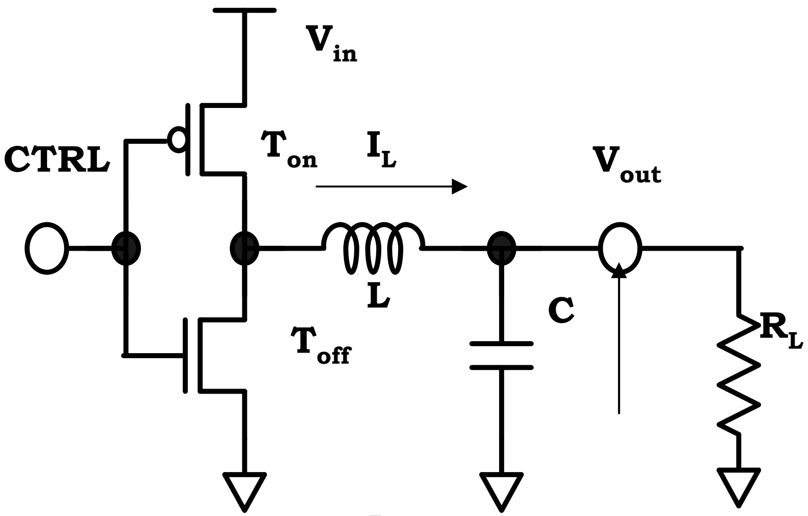
4 turns 85.6mm x 54 mm



T. Tanaka, et. al., Tech. Dig. of Int. 3D S I Conference, 6-1, 2007

マイクロ電力システム

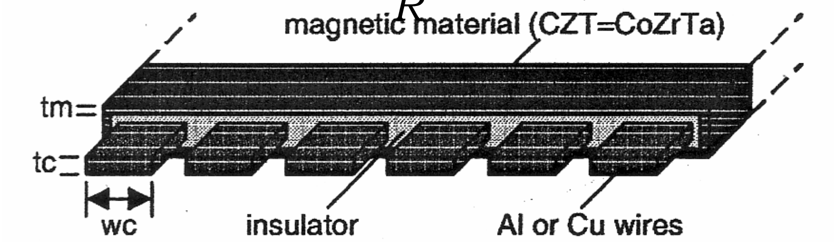
チップ上に電力供給システムを構築する動きが始まった。
低インダクタでも周波数が高ければ効率は高い。

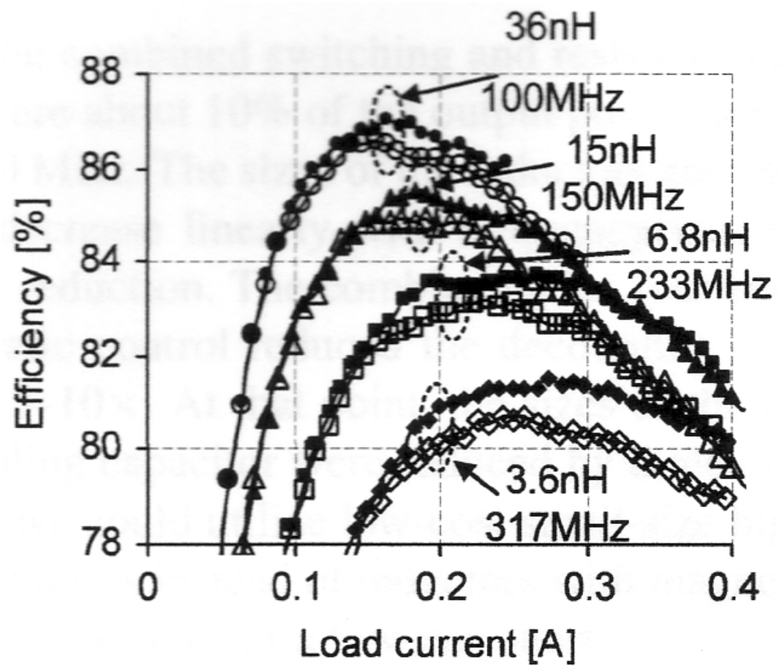


$$V_{out} = \frac{T_{on}}{T_{on} + T_{off}} V_{in} \qquad \Delta I_L \propto \frac{1}{Lf} \qquad Q = 2\pi \frac{fL}{R}$$

$$E_L = \frac{1}{2} L I^2, \quad P_L = \frac{f}{2} L I^2$$

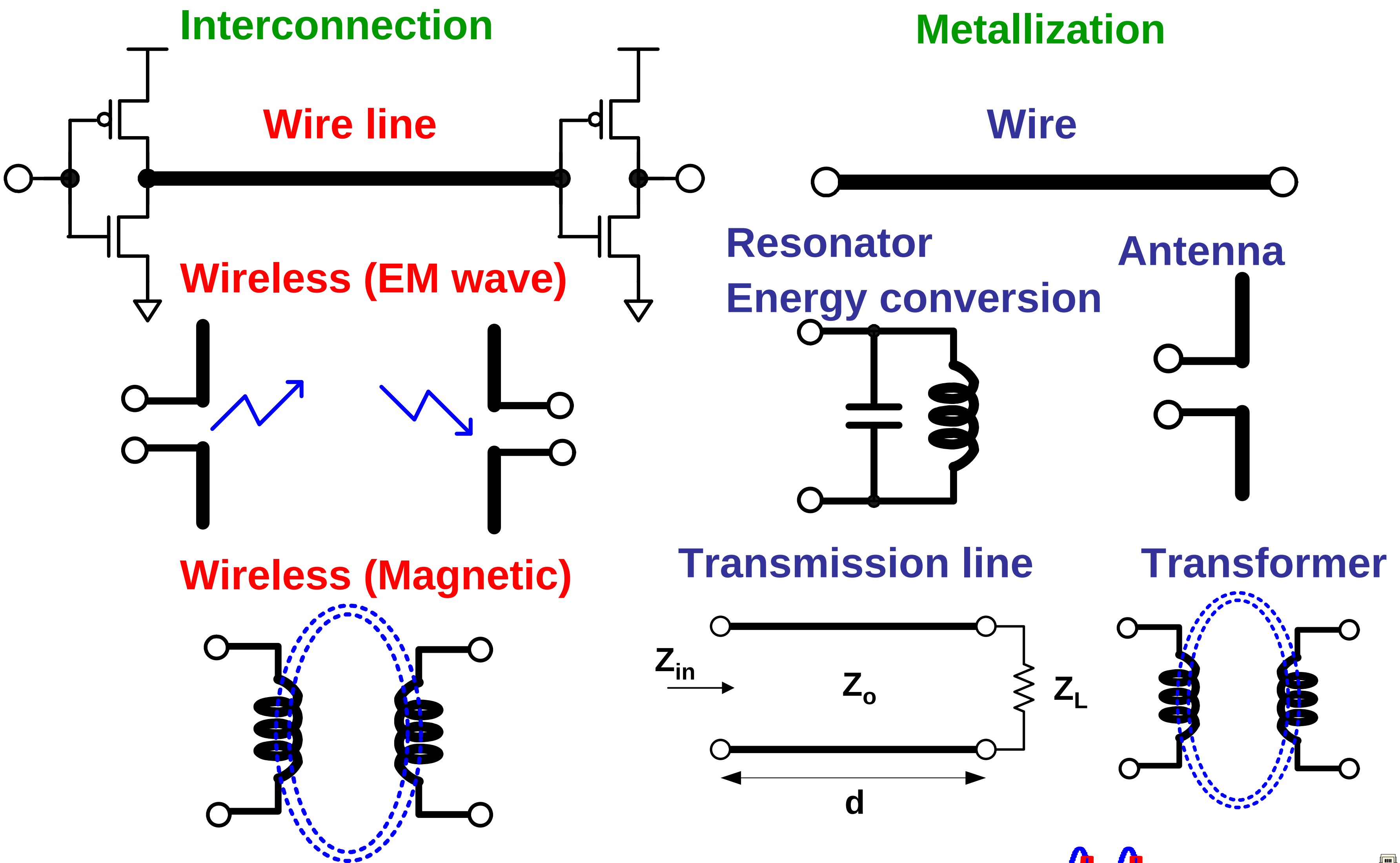
$$\mu_r = 900, \ \frac{L}{R} = 50ns$$





G. Schrom, et. al., Proc. ISLPED’04, pp. 263-268, 2004.

配線技術の様々な応用



Interconnection
Wire line
Wireless (EM wave)
Wireless (Magnetic)
Metallization
Wire
Resonator
Energy conversion
Antenna
Transmission line
Z_in
Z_o
Z_L
d
Transformer

まとめ

- RFCMOSの動向
  - インダクタをなるべく使用しない方向
    - 広帯域化
    - 省面積化　低コスト化
  - デジタルPAが出現
    - D/A変換技術をRF信号の発生に利用
  - サンプリングミキサー
    - スイッチと容量という準受動素子でMixerとFilterを実現
    - 離散時間信号処理技術がRFにも適用可能に
  - ミリ波SoCが出現
    - 130nm～90nmCMOSで60GHzが可能に
    - オンチップアンテナ
    - 位相差給電方式
    - 可変ビームフォーミング
    - オンチップレンズ
  - インダクタの応用が活発化
    - 近接データ伝送
    - 近接電力供給
    - オンチップDC/DC

結論：RF-SoCの動向

- **CMOSを用い、殆どのワイアレスシステムをワンチップに集積するRF-SoCの開発が進行している**
  - 大量品においてはRF-SoCがコスト的にも有利との見方
- **アナログ技術中心のRF-CMOSからデジタル技術中心のRF-CMOSに技術が転換し、成功を収めつつある**
  - アナログ技術中心：PVT、ミスマッチに弱く、性能、量産性ともに課題
  - デジタル技術中心：ばらつきに強く性能、量産性ともにクリアー
外部部品や調整箇所が少なく、コストも安い
- **RF回路にデジタル技術を適用するデジタルRF技術の開発が進められている**
  - アイデアはおもしろいが、性能は今一歩、さらなる技術開発が必要
- **ミリ波用途のRF-CMOS開発が台頭し、電磁波的回路のチップ集積が可能となり、新たな技術領域を拓きつつある**