

# Feed-Forward Compensation for All Digital Phase-Locked Loop based Synthesizers

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**Abstract:** Fast settling phase-locked loop based frequency synthesizers are necessary for fast frequency switching communication systems; for example in frequency hopping communication systems. Conventionally the loop filter's bandwidth is controlled to enable faster settling while maintaining low phase noise after settling. Feed-forward compensation is a perfect alternative candidate for all-digital phase-locked loop based frequency synthesizers. This technique is explored further here.

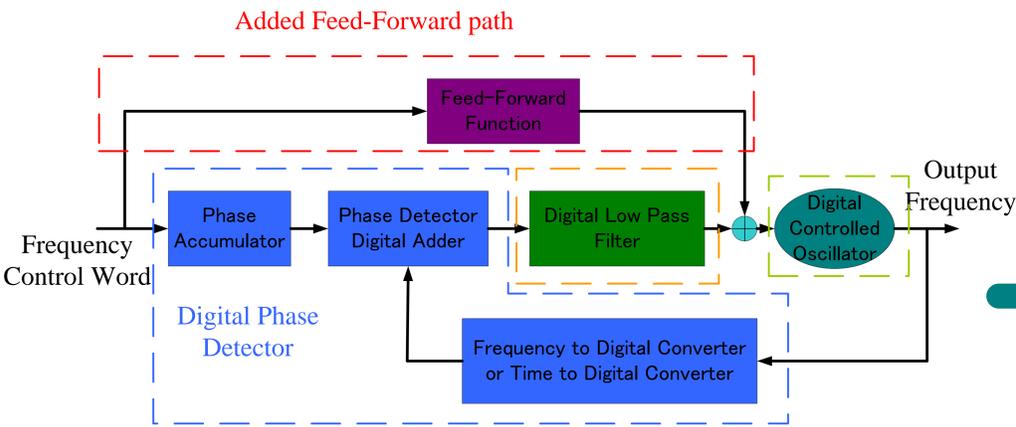


Fig. 1: All Digital Phase-Locked Loop with Feed-Forward Compensation

The output of the ADPLL without the feed-forward path can be shown to be related to the input by the following equation

$$\Delta f_v = \frac{(N \cdot F(z) \cdot K'_{DCO})}{f_R \cdot (z-1) + F(z) \cdot K'_{DCO}} \cdot \frac{\Delta f_R}{f_R} + \frac{f_{free} \cdot (z-1) \cdot f_R}{f_R \cdot (z-1) + F(z) \cdot K'_{DCO}}$$

With the Feed-Forward Path and setting the DCO scaling factor to the reference frequency  $f_R$  and complete compensation by exact prediction of DCO gain and offset

$$\Delta f_v = N \cdot f_R \cdot \frac{\Delta f_R}{f_R}$$

In reality however, this is not possible due to the finite precision of the digital circuitry, and error in gain prediction. With prediction and precision error, the system's response then becomes

$$\Delta f_v = \frac{\Delta f_R}{f_R} \cdot N \cdot f_R + \frac{\Delta f_R}{f_R} \cdot N \cdot f_R \frac{e_k \cdot (z-1) \cdot f_R}{(z-1) \cdot f_R + F(z) \cdot K'_{DCO}} - \frac{(e_k + e_f + e_f \cdot e_k) \cdot (z-1) \cdot f_R}{(z-1) \cdot f_R + F(z) \cdot K'_{DCO}} f_{free}$$

$\Delta f_v$	Output Expected Frequency	$K'_{DCO} = \frac{K_{DCO}}{K_{DCO}^{\Delta}}$	Normalized DCO gain
$N$	Frequency Multiplication Factor	$K_{DCO}$	DCO Gain
$\frac{\Delta f_R}{f_R}$	Input Frequency time step	$K_{DCO}^{\Delta}$	DCO Scaling Factor
$F(z)$	Low-Pass Filter Transfer Function	$f_R$	Reference Frequency
$f_{free}$	DCO Free Running Frequency	$e_f$	DCO Offset frequency prediction error
$e_k$	DCO gain prediction error		

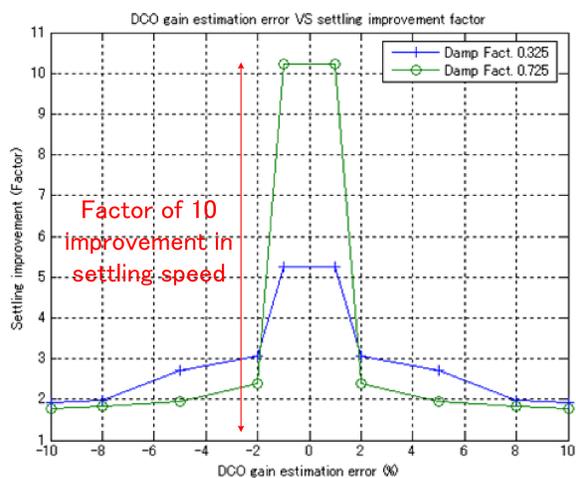


Fig. 5: All Digital Phase-Locked Loop Settling time improvement VS DCO gain estimation error

DCO's free running frequency  $f_{free}$  is found by breaking the feedback loop, inputting a '0' in the frequency control word, and measuring the output from the TDC/FDC

$K'_{DCO}$  can be found by measuring two input words to the DCO at different input frequency settings

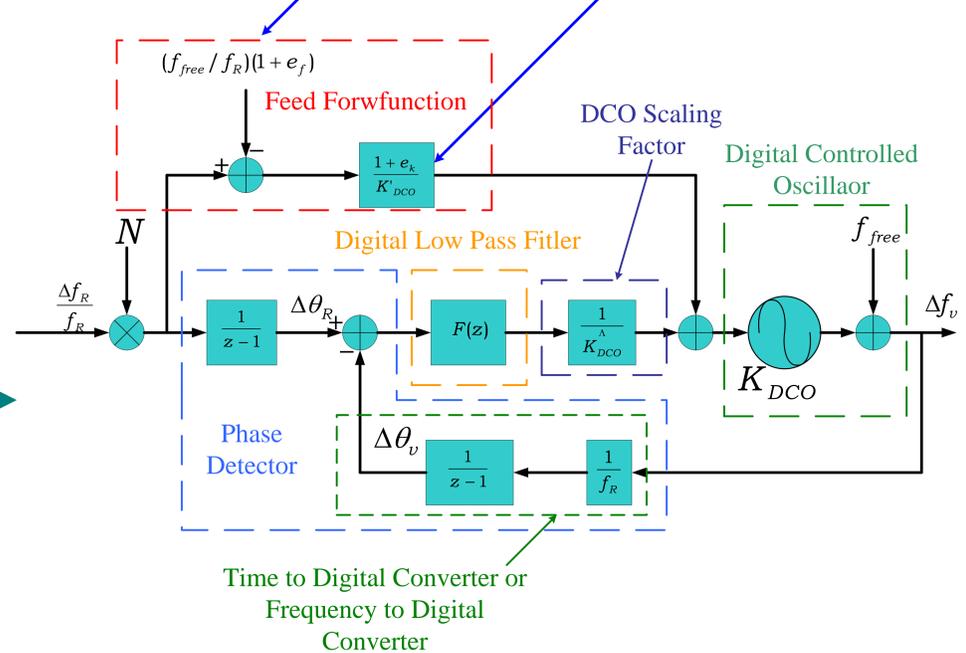


Fig. 2: All Digital Phase-Locked Loop Z-domain Model

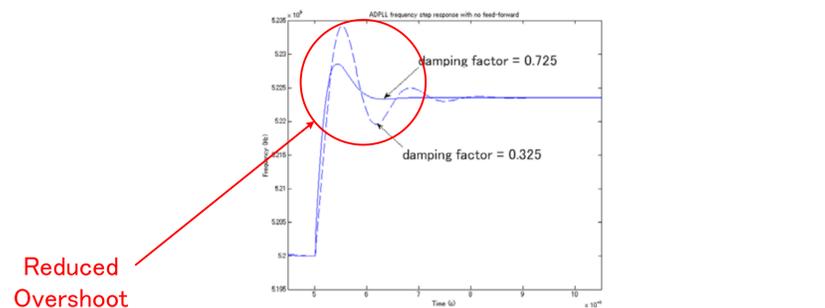


Fig. 3: All Digital Phase-Locked Loop Response without Feed-Forward Compensation

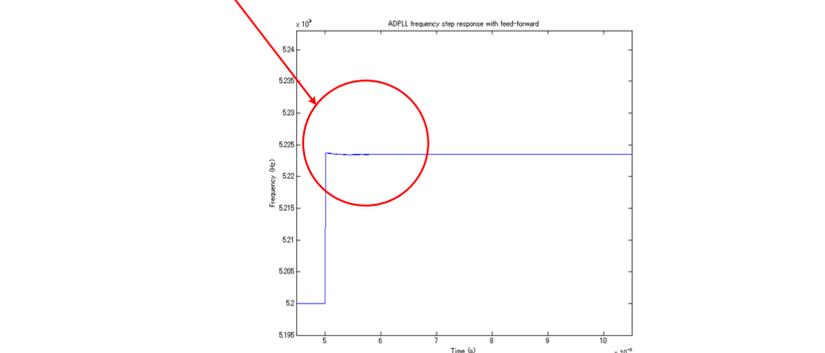


Fig. 4: All Digital Phase-Locked Loop Response with Feed-Forward Compensation

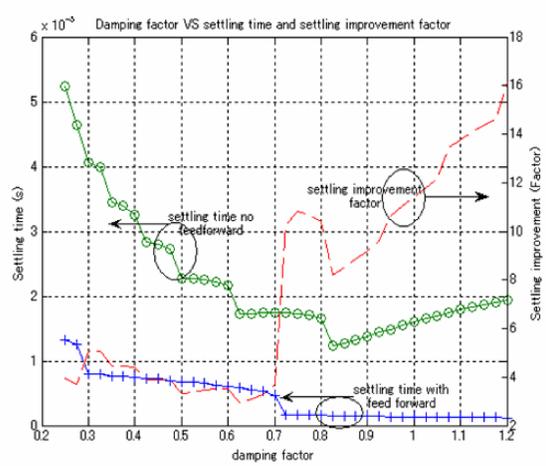


Fig. 6: All Digital Phase-Locked Loop Settling time and improvement factor VS damping factor at 1% DCO gain prediction error